A Low Power Dual Modulus Prescaler

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Abstract

CMOS refers to both, reduction in size and power consumption. Here, the Dual Modulus Prescaler is to be fabricated in 90 nm technology. It basically comprises of AND logic which controls the pulses produced at the output i.e. 1 or 2 pulses that need to be generated at the output, from 256/257 input pulses respectively. The synchronous divide-by-4/5 divider uses symmetric fashion D flip-flops with nMOS gates and the inverters to achieve more than 10 GHz maximum operating frequency. The use of this design will make the consumption of the power in microwatt, as the source couple logic used in the previous design concepts has power consumption in mW [1]. This modules output is to be carried out by using the Micro wind software 3.1. The prescaler will require 1.2-V supply. The prescaler's estimated operating frequency is upto 17 GHz.

*Keywords:*Dual modulus prescaler, CMOS, low power.

1. Introduction

With the expanding need in terms of the low power consumption and increasing frequency of operation, CMOS has been the key element to fabricate the components. Also, the highest operating frequencies of prescalers implemented in GaAs and SiGe bipolar technologies have reached 27 GHz [3] and 36GHz [4]. Bipolar technologies do offer a high range of frequency of operation but at the expense of power consumption. So, to minimize the power is of prime importance. The prescaler block do consists of various submodules which comprises of nMOS and pMOS. These transistors can be effectively used so as to reduce the area as well as the power consumption. The D flip Flop internal circuit is also shown here along with the waveform and the power consumption has been brought to 5.4 µW. Compared with these, the prescalers fabricated in CMOS processes usually operate at lower frequencies. The highest reported operating frequency for CMOS prescalers is 15GHz [6], [7]. The circuit has been fabricated in a 130-nm technology and consumes relatively high power (115mW).

Extra feedback networks were used [5] to increase the operating frequency to 14 GHz in a 0.18 µm CMOS process. A phase-shifting prescaler switches among signals with varying phases to achieve two or more divide ratios. The highest operating frequency for phase shifting prescalers [6] is 13 GHz and consumes 41 mW of power.

A dual-modulus prescaler is one of the complicated building blocks in phase lock loops.

The maximum operating frequency of prescaler sets the PLL. But when the question comes of power consumption, then we have to go with the CMOS technology. This design of prescalers has the focus on the reduction of the chip size and the power consumption. The design of low-power high-frequency divide-by N/N+ 1 dual modulus prescaler is a bit challenging.

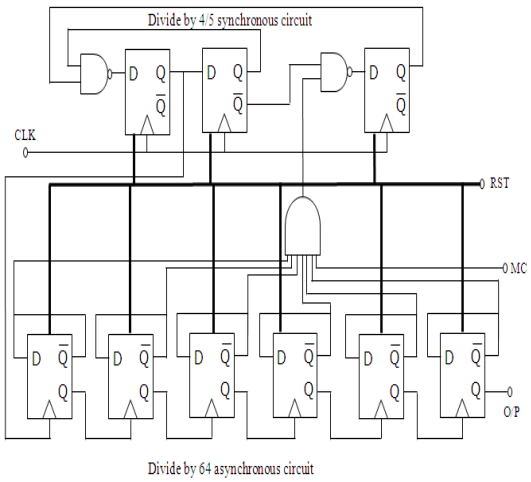

Fig. 1: A Dual Modulus Prescaler

The 90 nm technology will have the pull-up and pull-down pMOS and nMOS so that the signal strength does not become weak which forms the input to the AND gate for the extra clock pulse to get added i.e. 2 pulses at the output are produced. This paper presents a low-voltage low-power 256/257 dual-modulus prescaler. . The circuit is to be fabricated in a 90-nm CMOS process and voltage required is 1.2-V. This forms the main voltage that is given to the circuit. The equivalent resistance for the n-channel and p-channel transistors are given by:

$$R_N \alpha \frac{L_N}{W_N K'_N} \quad \ldots\ldots (1)$$

$$R_P \alpha \frac{L_P}{W_P K'_P} \quad \ldots\ldots (2)$$

Here, R= Resistance of the MOS,
L= Length of the channel,
W= Width of the channel,

2. The 1 pulse addition/ subtraction block

The dual-modulus prescaler consists of a synchronous divide-by-4 and divide-by-5 counters and an asynchronous divide-by-64 circuit as shown in Fig. 1**.** The output pulses are controlled with the help of mode control (MC) which is either set to low or high to get 1 or 2 pulses from 256 or 257 pulses respectively as the reference or input pulses. The main element is the synchronous divide-by-4/5 circuit because it operates at the highest frequency as the input or the reference frequency which is given from the master oscillator.

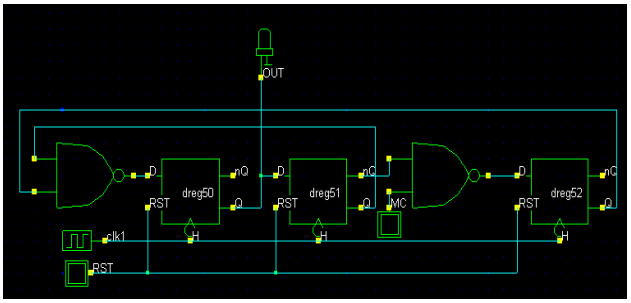

Fig. 2: The 1 pulse add/sub. block in DSCH

Also, we can add the reset logic so as to successfully put the entire system in the initial state. The circuit when gets a high pulse at the input of the 7 input AND gate, the pulses that the prescalers acts is 2 pulses that is when the total number of pulses are 257, at the input, then and then the final output will be 2 pulses. The condition reverses when the number of pulses at the input are 256 i.e. here the output of the 7 input AND gate is low, thus producing 1 pulse at the output.

Table 1. Estimated work with past work's comparison

Parameter	1994	2004	2012	Estimated Project work. (2012-2013)
Power consumption	25.5 mW	6.25 mW	3.84 mW	In µW
Technology	800 nm	130 nm	90 nm	90 nm
Flip flop	D & T f/f	D f/f	D f/f (SCL)	D f/f (Inverter & MOS only)
Supply Voltage	5 V	1.25 V	1.2 V	1.2 V
Capacitance effect	High	Med	Med	Least

2.1. *What's new in this?*

Due to the circuit complexity, the problem of area and capacitance effect is the major issue. So, to keep the spacing between two parallel vias is important. This spacing automatically increases the area. Also, if the number of components on chip increases, the area again increases and so the power consumption. A design of D flip flop is presented which consists of a fewer components to reduce the power consumption.

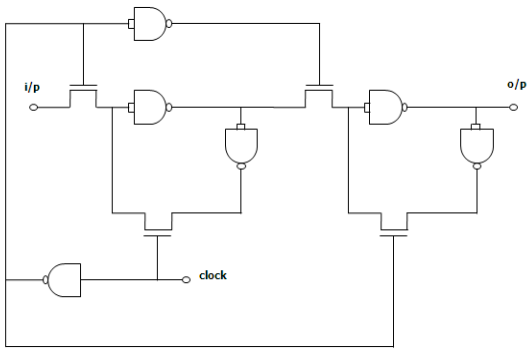

Fig. 3: A D flip-flop with NMOS and inverter

Fig. 3 shows the implementation of D flip flop used in the divide by-4/5 circuit. We have designed it using NAND, NOR or any other basic gate. But this is completely different. The circuit is like cascading of two similar blocks. Block one includes two nMOS and the first 2 inverters. The rest of the circuit is the repetition of the first part. Here, the circuit involves only two basic elements i.e. the nMOS and an inverter and the clock are of two types, one is clock and the next is its complement that is clk_bar. For that we need an extra inverter (inverters at the extreme top and bottom of Fig. 3). But while designing it in Micro wind, we are having clk and clk_bar. So, no need of that extra inverter.

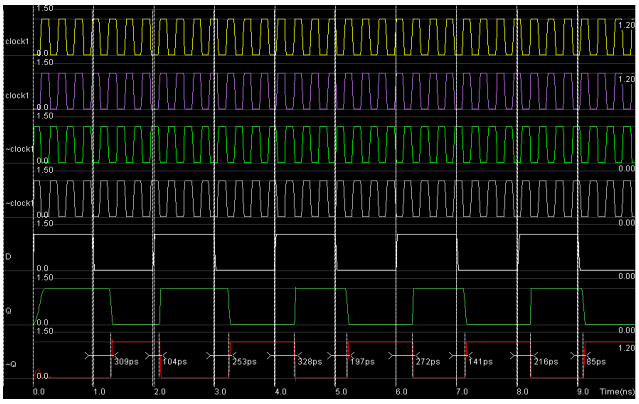

Fig. 4: Output of D flip flop

Here, the power consumption of the circuit in Fig. 3 is 5.420 µW if simple NOT gates are used.

2.2 *7 input AND logic*

This is used to select the number of pulses at the output i.e. if Mode Control MC=0, then output pulses produced are 1 and if MC=1, then output pulses produced are 2. the Fig. 5 shows the DSCH implementation of the same.

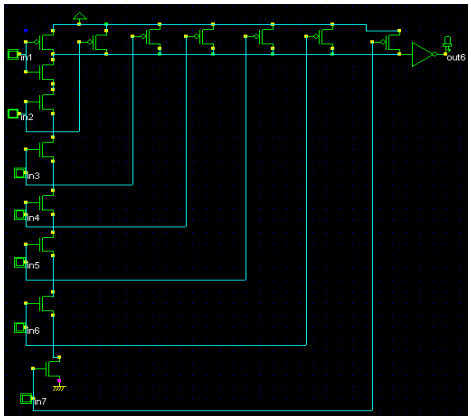

Fig. 5: 7 Input AND Gate in DSCH

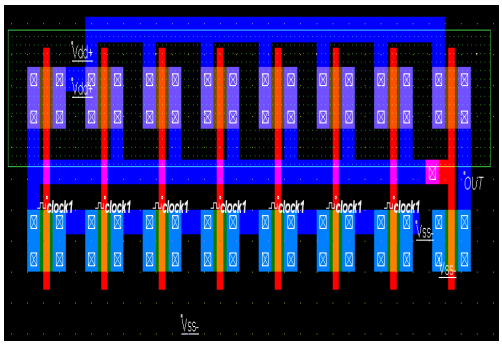

Fig.6: Layout of Seven input AND-gate in Microwind

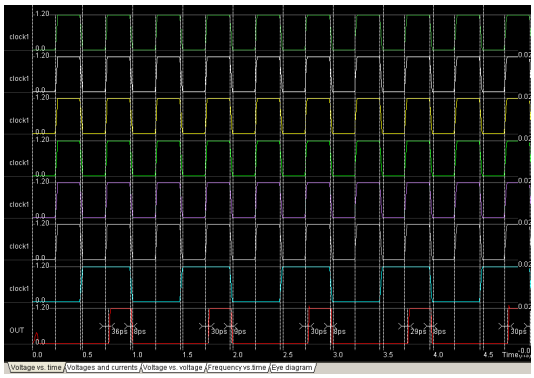

Fig. 7: Output of 7 Input AND Gate

The power consumption of the above circuit is: 4.9 µW and the technology used is 90 nm.

3. The Divide by 64 Unit

It is a chain of divide by 2 asynchronous counter. As per the Sequential Logic concept, D-type flip-flop can be connected together to form a Data Latch. Another useful feature of the D-type Flip-Flop is as a binary divider, for frequency division or as a "divide-by-2" counter. Here, the inverted output terminal Q (NOT-Q) is connected directly back to the Data input terminal D giving the device "feedback".

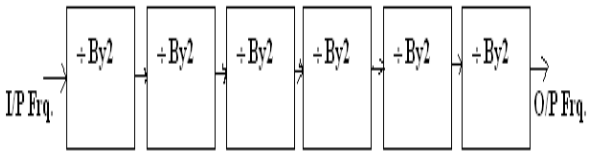

Fig. 8: Divide by 64

It can be seen from the frequency waveforms below, that by "feeding back" the output from NOT Q to the input terminal D, the output pulses at Q have a frequency that are exactly one half of the input clock frequency. In other words, the circuit produces frequency division as it now divides the input frequency by a factor of two.

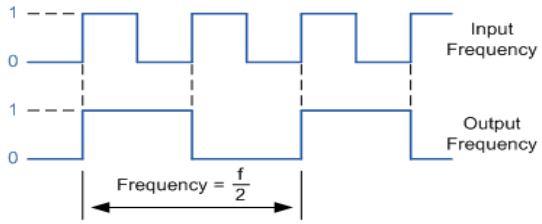

Fig. 9: Concept of divide by 2

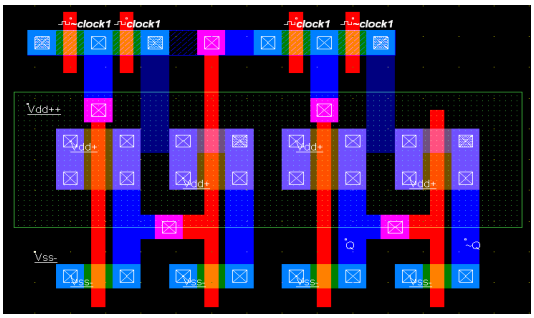

Fig. 10: Layout of Divide by 2 in Microwind.

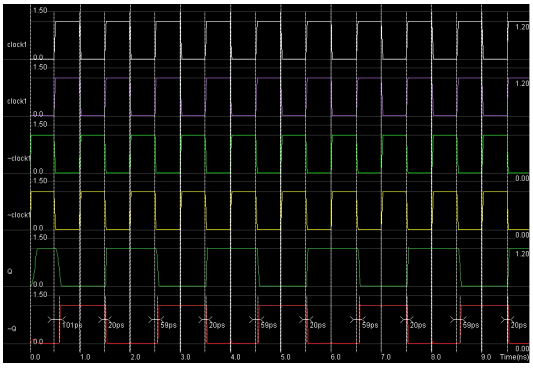

Fig. 11 : Output of Divide by 2

The output frequency Q and ~Q divides the input frequency clock1 by factor 2 .

Observations:-

Power consumption :- 6.056 µW.

Technology :- 90 nm.

Thus, the power consumption of the complete DMP will be upto 43 µW. This has been the least

power consumption reported for the 256/257 DMP.

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