High Speed Pipeline Multiplier Based on Re-configurable Voltage

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Abstract—**This paper bring forward a new high speed and efficiency Re-configurable pipeline multiplier, for the "bottle-neck" in signal process . The circuit was simulation under 0.25μm CMOS process. The circuit reduce the resource waste by 60 percent effectively and remain the high speed of 1.8GHz by control the voltage.**

Keywords—high speed, multiplier, pipeline

I. Introduction

Now multimedia communication is one of the key components of our life, and the variety rate signal process account for great proportion in video and audio signal process. the general multiplier in the variety rate signal process make the power waste graveness, and low efficiency. For this case, this paper design a Re-configurable, high speed pipeline multiplier for variety rate signal process, it has these characteristics that base on import frequency to control the work voltage and to control operation speed, such structure not only ensure the high speed signal but saving power greatly.

II. Multiplier Theory

General the non-sign number multiplication is to use binary system:

non-sign number X,Y

$$X = \sum_{i=0}^{M-1} X_i 2^i \quad Y = \sum_{i=0}^{N-1} Y_J 2^j \quad X_i, Y_j \in \{0,1\} \qquad (1)$$

Defining the multiplication

$$Z = X*Y = \sum_{k=0}^{M+N-1} Z_k 2^k = (\sum_{i=0}^{M-1} X_i 2^i)(\sum_{j=0}^{N-1} Y_j 2^j) = \sum_{i=0}^{M-1}(\sum_{j=0}^{N-1} X_i Y_j 2^{i+j}) \qquad (2)$$

In the digital design,hope the circuit frequency is more high,to ensure the data processing ability in the unit time. But the problem of delay is to restr and power waster ict the digital design[1],so we bring forward the pipeline structure.

III. High Speed Low Power Pipeline Multiplier

Generally,because "pipeline" can achieve high data rates at low supply voltages, so that can be use to extensive[2][3] . in this section we give background and describe the architecture of voltage re-configurable pipeline multiplier, it can carry out high circuit frequency and can to use lower voltage for reduce waste.

A circuit need least delay for correctness :

$$T_{\min} = t_{c-q} + t_{\max} + t_{su} \qquad (3)$$

t_{c-q} is transmit delay of register、 t_{su} is establish delay of register, $t_{\max}$ is the worst transmit delay, $t_{\max} = \sum_{n=1}^{N} \max t_n$.

If the circuit structure is pipeline ,the one clock work would been divided to N clock to do.the least delay is :

$$T_{MINPIPE} = t_{c-q} + \max(t_1, t_2, t_3...t_N) + t_{su} \qquad (4)$$

$\max(t_1, t_2, t_3...t_N)$ is the least delay in the N proportion[1].

In formula(3), $t_{\max} = \sum_{n=1}^{N} \max t_n$, The design of pipeline effectively reduces the delay of the multiplier to improve the operation speed.

A. Logic Design

2-bit re-configurable pipelined multiplier pipeline structure shown in Figure 1[1][3], Its have many electric voltage power supplies, adopting different work electric voltage under the signal condition of different velocity, to reduce consume.
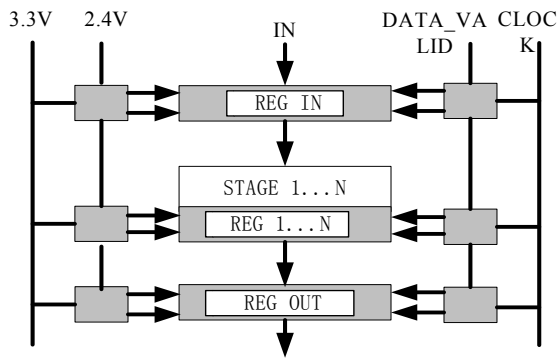
FIGURE I. PIPELINE MULTIPLIER LOGIC

B. Circuit Design

Multipliers are usually composed of three parts: generate partial product, partial product accumulated and the final results obtained[1].

1) generate partial product. Usually, partial product is the result of faciend and multiplier. This circuit will come into being four partial product: PP0,PP1,PP2,PP3, accumulate the four partial product to obtain the result.

$$PP_0 = X_0 Y_0 \qquad (5)$$

$$PP_1 = X_1 Y_1 \qquad (6)$$

$$PP_2 = Y_1 X_0 \qquad (7)$$

$$PP_3 = Y_1 X_1 \qquad (8)$$

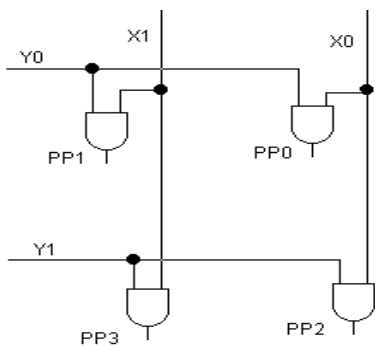figure 5 show the generate partial product:

FIGURE II. PARTIAL PRODUCT LOGIC

2) partial product accumulated. Generated the partial product, accumulate to obtain sum. Because the accumulate is a multi-operand addition, so to choose a effect adder is very important. But the multi-operand adder circuit implementation more complex, delay large, so the use of two operand adder[1].
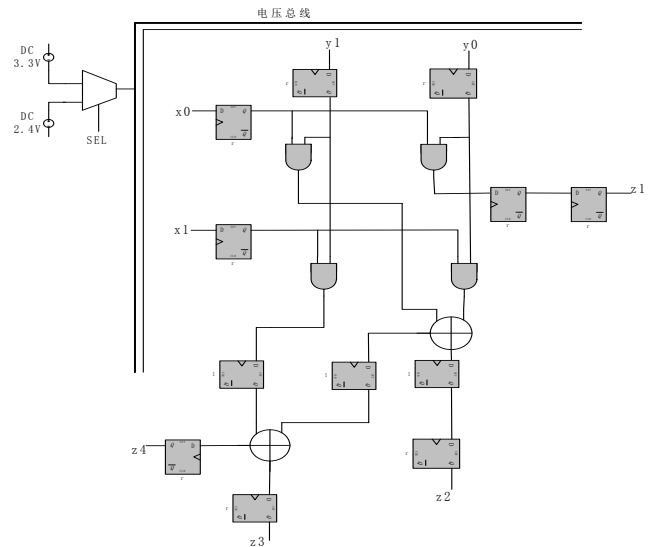
3) achieve circuit:

FIGURE III. TWO BIT MULTIPLIER CIRCUIT

Figure 3 show a high-speed two pipeline re-configurable two-bit multiplier circuit. Rising edge of the circuit using D flip-flop as a valid input and output registers[4][5]. And compared to the without pipeline multiplier, the multiplier greatly improves the operation frequency, however, use of "pipeline", although they can significantly increase the frequency of the circuit, but the high computing power accompanied by an increase in frequency. But also in signal processing is usually the maximum frequency as a standard treatment frequency, but the input frequency is generally much lower than the highest frequency, it is a serious waste of resources.no matter what the optimization of circuit structure in the depth of pipeline, or as little as possible increase components in the number, to use registers will increase the use of the circuit power.

In view of this, this paper designed a method of proportional reduction in power supply voltage, when the input data rate lower than the maximum processing frequency of the circuit, in accordance with the percentage of input data rate lower than the maximum processing circuitry to reduce the of frequency of power supply voltage to achieve an effective reduction in power consumption purposes. However, improving the circuit performance, the use of this technology the cost is relatively small, cost-effective high.

IV. SIMULATION

Figure 3 shows a Two step pipeline of two-bit multiplier circuit to be simulated. The circuit in two step pipeline, the use of Spectre simulation in 0.25μm standard CMOS technology (3.3V supply voltage). The output waveform shown in Figure 4, the figure in the first three clock cycles is preparation clock, valid output starting from the fourth clock cycle, can achieve the highest frequency of 1.8GHz
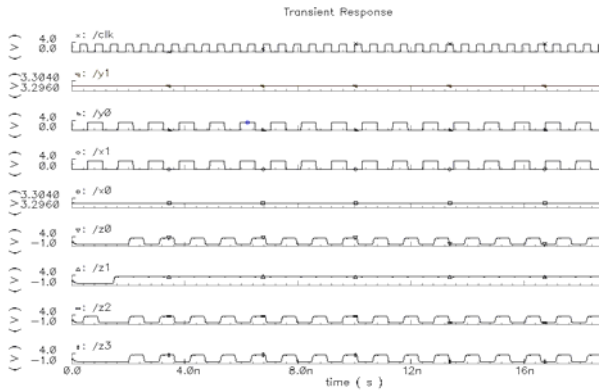
FIGURE IV. 3.3V POWER TWO BIT MULTIPLIER MULTIPLIER WAVEFROM

When a high-speed pipelines two-bit multiplier circuit as shown in Figure 4, whose frequency same as without pipeline for two-bit multiplier circuit with a maximum frequency of 1.2GHz, the use of Spectre based on 0.25μm standard CMOS technology simulation , its minimum supply voltage can be reduced to 2.4V, the minimum input signal voltage can be reduced to 1.5V the output waveform as shown in Figure 7.
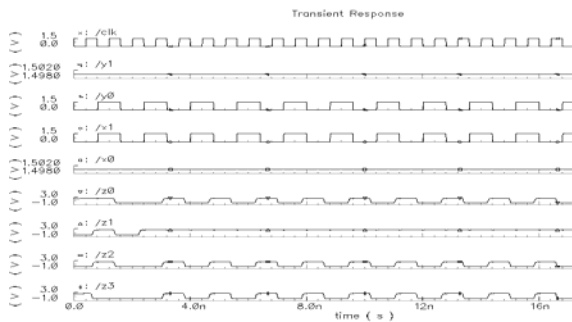

FIGURE V. TWO BIT TWO PIPELINE RE-CINFIGURABLE MULTIPLIER OF 2.4V VOLTAGE MULTIPLIER WAVEFROM

When the circuit frequency is 1.2GHz, its minimum supply voltage can be reduced to 2.4V, the minimum input signal voltage can be reduced to 1.5V, power dissipation can be reduced to 9.3mW,, compared to the circuit without pipeline when the frequency of 1.2GHz Power consumption reduceing by about 47%.

In particular, when the average high-speed pipeline multiplier processing the low-speed signal, the output of the effective clock cycle same as the input data clock cycles. This clock cycle includes many of the same clock cycle and clock cycle operation, that is the equivalent of a number of computing cycles is only the workload of an effective clock cycle, thus doubling the circuit waste of resources.

Pipeline multiplier can according to the frequency of the input signal, adjust the circuit supply voltage, greatly reducing the power consumption of the circuit. In this paper, the two-bit pipeline multiplier, for example, such as the input data is less than 1.2GHz choose to 2.4V power supply voltage, when the input data is more than 1.2GHz is less than 1.8GHz, select the 3.3V supply voltage. Using this method to build a number of pipeline can have a multiplier means that the frequency range

of more selective, circuit speed and the input signal rate is more match, save more circuit resources. Moreover, in dealing with different data rate signals using different pipeline series can also be improved to reduce power consumption in order to improve the circuit performance.

V.   CONCLUSION

This voltage Re-configurable, High Speed Pipeline Multiplier have this advantages with a flexible structure, high frequency, low power consumption, compact structure. May be different according to the frequency of the input signal, adjusting the power supply voltage of the circuit, can be a great and effective power saving power. In this paper, the two-bit pipeline multiplier, for example, such as the input data is less than 1.2GHz choose to 2.4V power supply voltage, when the input data is more than 1.2GHz is less than 1.8GHz, select the 3.3V power supply voltage, maximum reduction power consumption of about 46%.

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