

# 3D Simulations of Electrical Characteristics of Interleaved Shell-Electrode Detector

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**Keywords:** 3D Simulations, Interleaved Shell-electrode detector, Low electric field region; **Abstract.** An Interleaved Shell-Electrode Detector –ISED (Chinese patent #zl201721077852.6), based on the Closed Shell-Electrode Detector (CSED), is proposed for the improvement of charge collection efficiency by reducing the dead region. The novel design concept of ISED will be discussed in detail. Full 3D simulations of detector electric properties including profiles of electric potential and electric field have been carried out using a SILVACO TCAD tool. The dead region introduced by interleaved shell electrodes in an ISED single cell (the unit cell) that can form an effective array is half of that in a CSED. The disturbance of the electric properties by introducing interleaved shell electrodes in an ISED is minimum and kept in two localized corners in a square shaped single cell. Other detector properties such as detector full depletion voltage, capacity, breakdown voltage, and I-V and C-V characteristics have also been simulated, and results will be given.

#### Introduction

Silicon detectors are applied in high-energy physics and astrophysics due to its fast response speed, high sensitivity and radiation tolerance <sup>[1]</sup>. 3D column electrode detectors, with much improved radiation hardness as compared to 2D planar detectors, were proposed by Parker <sup>[2]</sup>. However, it was found that the electric field at the geometric center of electrodes is always low due to the symmetry of these electrodes. To overcome this problem, BNL proposed a 3D-trench electrode silicon detector in 2009<sup>[3]</sup>. However, since trench electrode in a 3D-Trench electrode silicon detector cannot be etched through all the way (otherwise the detector cell will fall off the wafer), there will be a low field region which occupies about 10% of whole volume at the bottom of the detector (the unetched part). This low field region give rise to some shortcomings of the detector, chief among them is that this low field region is a region with low charge collection efficiency due to long tail in the signal due to the low electric field. Slow drifting of carriers is to increase the drift time, and therefore increase trapping, constituting as an effective dead region in the low field region. So, it is necessary to reduce the low field region to cut down the dead region to improve charge collection efficiency.

To reduce the portion of low-electric field region and improve the charge collection efficiency of the detector, a new structure based on Closed Shell-Electrode Detector (CSED) [4] — interleaved shell-electrode detector (ISED) is proposed in this paper. The portion of the dead region is just half of that of CSED according to geometric calculations. In this paper, the following will be carried out:

1) design concept and 3D Structure of the ISED; 2) the simulations of detector characteristics using a SILVACO TCAD tool, including profiles of electric field and electric potential, the detector full depletion voltage, breakdown voltage, capacitance, and leakage current. It will show that the ISED has excellent electric characteristics with much smaller size of dead region than CSED.



## **Design Concept**

The structure of the proposed new ISED device, as shown in Fig.1a, is a PIN junction. In a unit cell, the central column electrode is surrounded by a trench electrode. P-type silicon with resistivity of  $1\times10^{12}/\text{cm}^3$  was selected as the material for the I part in our case, since p-type Si will not undergo the space charge inversion (n-type Si will invert to effective "p"-type) in high radiation influence environment <sup>[5]</sup>. Due to the asymmetry of ISED detector electrodes, maximum electric field in an ISED with the junction on the trench electrode is much smaller than that with junction on the center column. We thus chose the formal case to keep the maximum electric field down and therefore increase the detector breakdown voltage <sup>[6]</sup>. The electrode spacing of 20  $\mu$ m-100  $\mu$ m will help to enhance the hardness of the detector under high irradiation influence <sup>[7]</sup> ( $F \ge 1\times10^{14}\,\text{N/cm}^2$ ). Therefore, ISED with the electrode spacing  $\lambda$  of 35  $\mu$ m, p-type Si for I part material, and the outer junction (junction on the trench electrode) are chosen for this work for simulations. A 3D structure of ISED single cell is shown in Fig.1a. The thickness of the detector is d=200  $\mu$ m. The thickness of the n\*-type square trench is  $L_{\rm H}$ =30  $\mu$ m. The doping concentration of the p\*-type central column is  $10^{19}/\text{cm}^3$ , and again the doping concentration of the p-type bulk is  $10^{12}/\text{cm}^3$ .

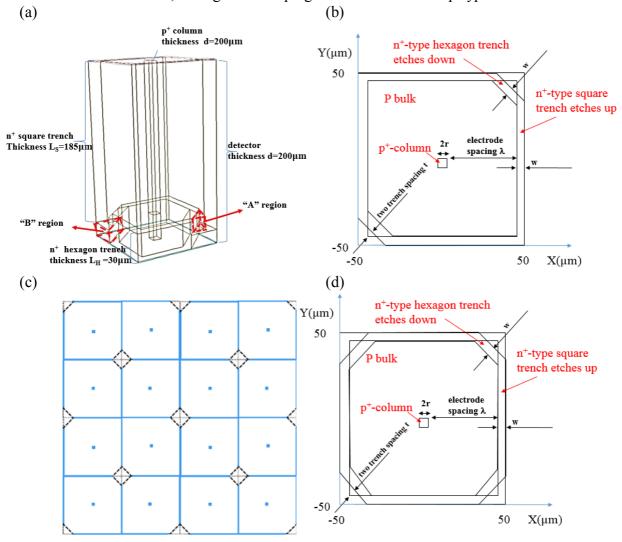


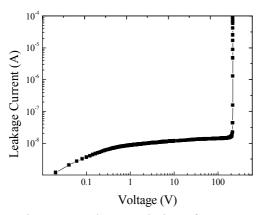
Fig. 1. a) a 3D structure of ISED single cell; b) the ISED single cell from the top view; c)  $2\times2$  array of ISED unit cell ( $4\times4$  array of ISED single cell) from the top view; d) the CSED single cell (unit cell) from the top view.



Fig. 1b is the ISED single cell from the top view. From Fig. 1a and Fig. 1b we can see that the trench electrode of an ISED is composed of a non-etching-through square shape trench etched from the top side and a non-etching-through hexagon shape trench etched from the bottom side. These two non-etching-through trenches are interleaved together in the vertical direction, overlapping in most parts except the opposite corners. The width of all trenches is w=10 µm and the width of central column is 2r=10 um. The maximum spacing of two trenches is t=10 um. An etch-through central column, together with the interleaved trench electrodes, form a single cell of ISED. Other than the two un-overlapped corners, the overall trench electrode is effective etch-through, thus effectively eliminating the dead region as existed in a CSED cell. Fig. 1c is the ISED unit cell from the top view, the thin dashed line represents square trench and the thick dashed line represents hexagon trench while the thick solid dots represent the etch-through region where the trench etched from the top overlaps the trench etched from the bottom. From Fig. 1c we can easily know that the thick dots are not closed when four ISED unit cells arranged in a mirror array (to form a unit cell). From a unit cell, one can easily make a detector array as shown in Fig. 1c. As we can see, since all the trenches are not closed, the detector bulk can never fall off the wafer. From Fig. 1a, we see that "A" regions are regions between hexagon trench and square trench while "B" regions are regions under the square trench (in Z direction) while in the outside of the hexagon trench in r direction (as shown in Fig. 1a). Each single cell is connected through "A" regions and "B" regions to the detector chip to form the mechanical integrity (not fall off). Free carriers generated by MIP particles in the "A" region and "B" region cannot be collected since the electric field is very low in these regions and octagonal trench is acted as a barrier during the drifting of the carriers. This is why "A" regions and "B" regions are called dead regions. From Fig. 1b to Fig. 1c we can see that two "A" regions and two "B" regions in a single cell of ISED, while four "A" regions and four "B" regions in a single cell of CSED. Obviously, the total volume of dead region in ISED is only half of that in CSED.

## I-V and C-V Characteristics of the Interleaved Shell-Electrode Detector

Fig. 2 is the simulated I-V curve of an ISED. The detector is fully depleted at about 1 V ( $V_{fd}$ =1) with a breakdown voltage ( $V_{br}$ ) of 214 V. We note that the value of  $V_{br}$  is two orders of magnitudes larger than that of  $V_{fd}$ . The stable leakage current is 1.5×10<sup>-8</sup>A, as shown in Fig. 2.



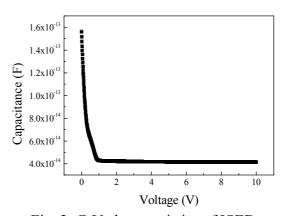


Fig. 2. I-V characteristics of ISED

Fig. 3. C-V characteristics of ISED

Fig. 3 shows the simulated detector C-V characteristic of an ISED. As shown in Fig. 3, the detector capacitance decease with approaching to a certain value of 40 fF, which is the detector geometry capacitance.

#### **Electric-Field and Potential Profile of the Interleaved Shell-Electrode Detector**

The electric field distribution of a detector in the working condition affects the detector's performance. Carriers will drift faster and be harder to be trapped by the deep level defect if the



electric field is high. The charge collection efficiency will be better when the carrier drift path is a straight line since the distance of the straight line is always the shortest <sup>[7]</sup>.

From Fig. 4a, we can see that the electric field distribution is uniform in the vertical direction of ISED. In the bottom areas, the electric field (E) is high, enabling carrier drift to the collector in a fast speed, which is why ISED is better than 3D trench electrode detectors <sup>[3]</sup> in charge collecting efficiency. From Fig. 4b, the Z component of E (E<sub>Z</sub>) in most regions of the detector is 0, indicating that in most regions the carriers only drift in the X-Y plane and the drifting path is always a straight line. E<sub>Z</sub> is not 0 at the bottom of square and the top of hexagon, where the PN junction is formed between the n+-type Si and P-type Si. E<sub>Z</sub> is 0 in the "A" region where square and hexagon is interleaved thus the carriers in the "A" region will only drift in the X-Y plane and holes will never drift to the center electrode, indicating there is hole shielding effect in the outer side of hexagon. Even though those carriers are drifted from "B" region to "A" region under the influence of E<sub>Z</sub>, they will not be collected by the center electrode due to the hole shielding effect, that is why "A" region and "B" region are called dead regions. It is worth to be noticed that E<sub>Z</sub> component is existed near the surface, and it is caused by the boundary.

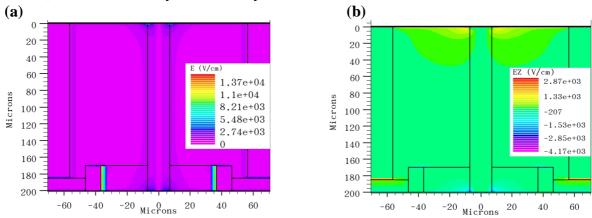


Fig. 4. Electric field profile of ISED: a) electric field profile in Z direction; and b) distribution of Z component of electric field in Z direction.

## **Summary**

A new type of detector, ISED is proposed for the improvement of the charge collection efficiency and the reduction of the dead region. The design concept and the specific set of parameters have been described in detail. The dead region occupies 15% of 3D-trnceh electrode silicon detector, 0.3% in CSED while just 0.15% in ISED. Through the analysis of simulation results from SILVACO TCAD, it is concluded that the stable capacitance is very low at about 40fF. The detector full depletion voltage has been found to be about 1 V, which makes it possible to operate the detector at a voltage of about a couple of volts. Moreover, since the detector breakdown voltage is found to be 214 volts, much larger than the detector operation voltage of a few volts, it is virtually impossible to breakdown the detector.

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