A 16b 4GSPS Two-Times Interleaved DAC with INL≤±2.9LSB

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Abstract. A two-times interleaved DAC in a standard 65nm CMOS technology is presented with a data-clock frequency of 4GHz with INL<±2.9LSB. Since two DACs are placed in parallel, their output current goes to the DAC multiplexer, which alternatively connects one DAC to the output, and the other one to an identical dummy output. The two-times interleaved DAC with quartered switches increases the overall data of two times and reduces the complexity of the design effectively while suppressing the non- idealities.

1. Introduction

With the continuous improvement of data rate, the difficulty in ultra-high-speed single-core DAC designing has been difficult for hardware designers to accept. The dynamic errors and static errors affect the performance of ultra-high-speed DAC seriously, in which the impact of dynamic error is particularly prominent [1].

In this paper, the dual-channel core parallel output architecture is presented requiring a two-times interleaved structure to combine the two outputs into one output. This structure seems to increase the chip area and the power consumption, but it suppresses the dynamic non-ideal effect in the DAC cores, and simplifies the structure designing of a single DAC core, which corresponding reduces the chip area and power requirements[2]. Overall, the design of the two-times interleaved structure solves the problems in ultra-high-speed DAC.

2. Architecture

The following figure shows the block diagram of the two-times interleaved DAC. The current-steering is used in two sub-DACs, and each sub-DAC contains a current source arrays, cascode, differential output switches, switch drivers and peripheral circuitry about the clock.

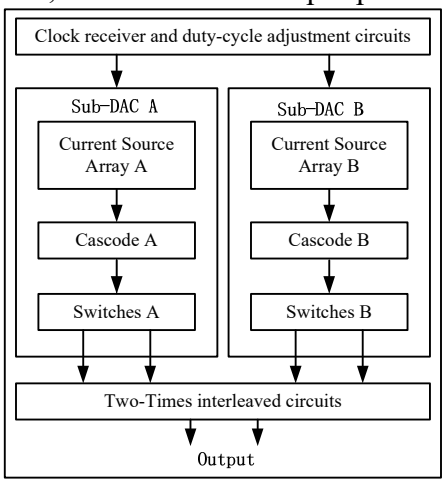

Fig.1 The block diagram of the two-times interleaved DAC

Communication usually requires the accuracy of DAC range from 12 to 16 bits. The minimum current source is not realistic, because it needs 4K-65K drive units. So the segment structure is presented. In this paper, the high-6 bits of each sub-DAC adopts decoding technology with dynamic cell matching (DEM) and the low-10 bits of each sub-DAC adopts the binary decoding segment structure, so that the current source array of each sub-DAC consists of 64 MSB current sources and

10 LSB current sources. Each sub-DAC receives 16-bit 2GS/s external data DATA_A and DATA_B with phase difference of 90 degrees. As shown in Figure 2, the sub-DAC will generate the non-return-to-zero current output waveform. The current will be resampled by the clock, and the clock will select the stable current signals in half a cycle as return-to-zero (RZ) waveform[3]. Since the RZ waveform has an amplitude attenuation of 6 dB, two sub-DACs are required with 180 degrees phase difference. So that the complete non-return zero (NRZ) output waveform is synthesized[4].When the sub-DAC switches process the next code, their outputs are connected to the dummy outputs. So the momentary dynamic errors of the switches flow into the dummy outputs so that the non-ideal effect does not transmit to the DAC output. When these errors meet the stable output requirements, the analog current switches are connected to the output of the sub-DAC, during which the other sub-DAC processes the next code and is connected to the dummy output. Although the two-times interleaved DAC consumes a certain amount of power and area, this will reduce the requirements for timing and settling time in DAC, and power consumption can be controlled to an acceptable level[5][6].

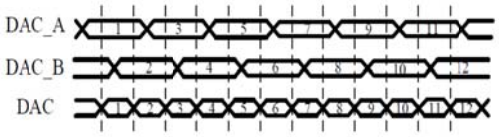

Fig. 2 Digital phase relationship

2.1 Quartered switches

Figure 3 shows a switching scheme of code-independent current switch. Replacing the traditional dual-differential switches with the quartered switches, each switch is controlled by a control signal. The four control signals will further improve the dynamic characteristics of the ultra-high speed D/A converters. The four control signals are derived from the logic values of the input data and the clock signal. As a result, when the data dose not change in two successive clock cycles, the clock produces the changing data on the four switches, but the changing data does not cause a change to the output current. When the data changes in two successive clock cycles, the switches change in phase with the data value, thereby causing a current output.

The timing diagram is shown on the right. It can be seen that the signals on the current switches are constantly complementary regardless of data changing or not, and the pattern does not change with the data model. Thus, the glitch associated with the code data is converted into a fixed-frequency spurious tone which is a high frequency of 2 times to the clock. So the spurious tone is far from the usable signal band and it is easily filtered out.

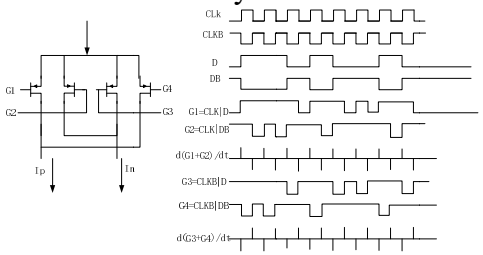

Fig.3 Code- independent current switch

2.2 Two-times interleaved circuit

The two-times interleaved circuit structure is shown in Figure 4. The two parallel DAC cores, I and Q, are current-steering. The clock signals control the on-off of the interleaving switches, so that the analog output signals of two channels are alternately conducted to the DAC output and dummy output, achieving the dual-channel two-times interleaved output.

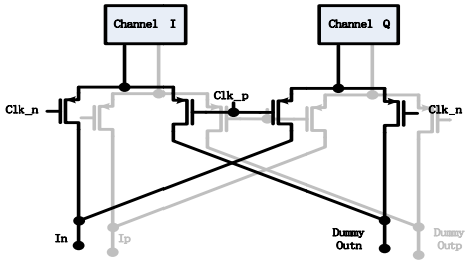

Fig.4 the two-times interleaved circuit

In this paper, the dual-channels two-times interleaved technique is adopted to realize the high sampling frequency of 4GSPS. Analog domain of the dual-channels two-times interleaved technology is shown in Figure 5. By interleaving the two analog signals from channel A and B with the same sampling frequency as f_{DAC} and 180 degrees of phase difference, the overall sampling rate of the interleaved DAC is equivalent to 2 * f_{DAC}.

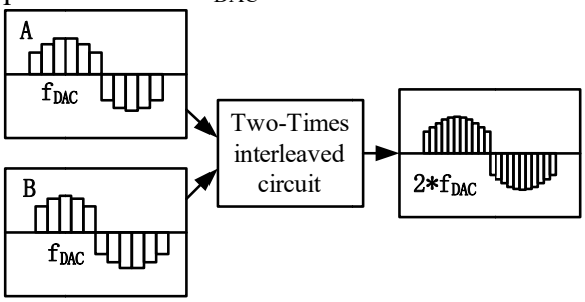

Fig.5 Analog domain interleaving

2.3 Clock receiver and duty-cycle adjustment circuits

In a two-times interleaved DAC, the time for sub-DAC which is connected to the DAC output must be the same with the other one. Otherwise an offset error and a timing error will be introduced. The glitch will appear around the half-Nyquist frequency in the frequency domain, affecting the output bandwidth of the DAC. When the timing error is present at t, the spurious-free dynamic range (SFDR) is said as follows:

$$\mathrm{SFDR} = 20\log_{10}\left(\frac{1}{\Delta t * \pi f_{signal}}\right)$$

This relationship indicates that the static timing error must be less than 500fs, while the sampling rate is 4GS/s, SFDR> 50dB within the full Nyquist zone. This level of accuracy can be met by calibrating and adjusting the clock. The clock module comprises a clock receiving circuit, a frequency dividing circuit, a duty-cycle adjusting circuit and a driving circuit. The clock receiving circuit is shown in Figure 6. Using the CML architecture it supports clock frequencies up to 10 GHz, a 50 Ω resistor is connected to a 1.2V source in parallel on each receiver pin to produce a differential signal. Then the internal CML receiver receives the external clock signal, and the shifter converts the CML signal to the CMOS signal. The duty-cycle of the clock can deviate by 50% as the manufacturing process and temperature deviating. We calibrate the timing by DC measurement. One of the two sub-DACs is firstly set to the maximum output swing, and the other is set at the minimum output value. The average output voltage depends on the amplitude of the signal and the duty-cycle of the square wave received. The timing alignment circuit adjusts the clock edge through the capacitors which are controlled digitally in Figure 7 until the duty-cycle approaches 50%.

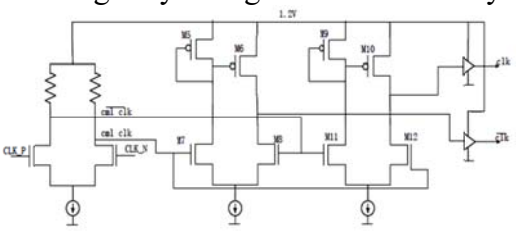

Fig.6 Clock receiving circuit

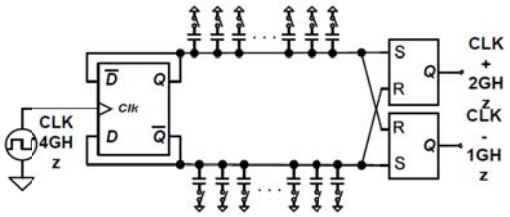

Fig.7 duty-cycle adjustment circuit

3. Measurement Results

Inputting ramp data, the simulation results are as follows:

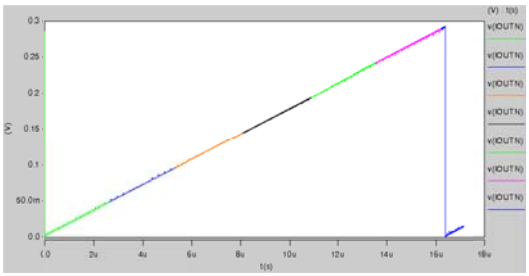

Fig.8 Ramp simulation results

DNL and INL test results are as follows, where DNL is ± 1.8LSB, and INL is ± 2.9LSB:

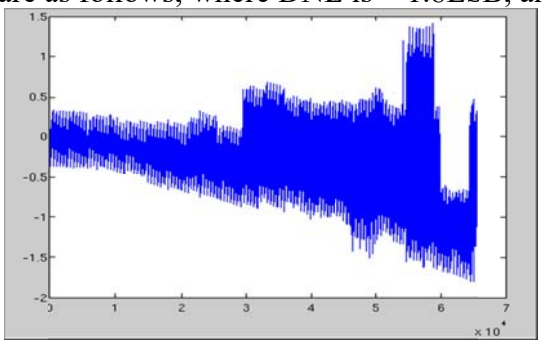

Fig.9 DNL test results

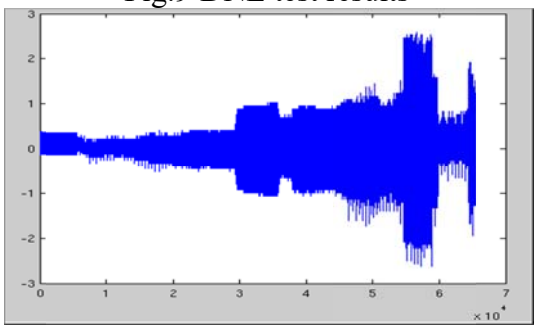

Fig.10 INL test results

4. Conclusions

Through the two-times interleaved circuit, the DAC conversion rate is greatly improved, and the design problem of the ultra-high-speed DAC is solved. Simplifying the design difficulty of the ultra-high-speed DAC, it effectively reduces the overall area and the power consumption.

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