

## A Low Power Implementation Strategy for SOC

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**Abstract.** Low power consumption has become an extremely important design goal for system-on-chip(SOC). This paper analyzes the impact of power consumption on the digital chip and the composition of power consumption in the circuit, and then proposes a low-power implementation strategy for SOC system with embedded multi-core CPU. A master-slave control circuit is designed to reduce the static and dynamic power consumption of on-chip CPU and on-chip functional modules. Which not only improve the SOC chip on the functional modules and multi-core CPU switch flexibility, you can also reduce the total SOC system chip power consumption.

### Introduction

Now the world are advocating the concept of green technology, energy conservation, power consumption requirements of the IC is the smaller the better. The problem of chip power consumption has been paid more and more attention in recent years, mainly comes from: With the development of deep submicron chip technology and design flow, the integration degree of the chip has reached one million gate level, the scale is more and more big , Function more and more, which produced a chip packaging costs, power supply costs and reliability issues. If the SOC chip power consumption is too large, will produce the following hazards:

- l Energy consumption;
- l limit the use of battery time;
- l increase chip manufacturing costs, heat problems become very serious;
- l reduce chip reliability;
- l limit chip performance;
- l impact on high-performance digital SOC system design and market applications.

Therefore, we must carry out deep sub-micron low-power technology to meet the user's power consumption requirements of the chip.

Figure 1 shows a communication device system, the application of low-power SOC. In the system to achieve master-slave control, in which the Intel CPU in the master position. SOC in a subordinate position to achieve the master CPU information Receiving response, control of other subsystems in the communication device, and realizing CAN, UART and other information

transmission connection with other communication systems through the interface. The system of the SOC low power requirements are high, and requires a number of SOC internal modules (including on-chip functional modules and on-chip CPU) is not used when turned off, and can be Intel CPU wake up to the main controller of the flexible control .

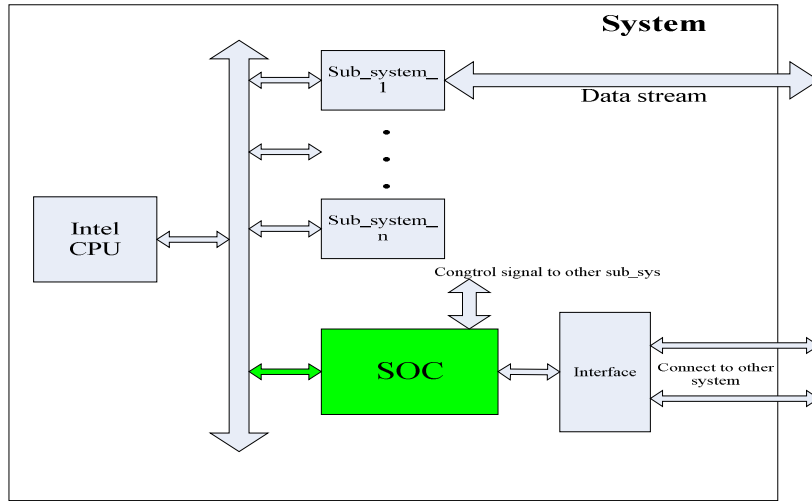


Fig. 1. The architecture of a communication system using a low-power SOC

In order to achieve this kind of master-slave control of low power consumption requirements, this paper analysis and consideration from the CMOS power structure, low power consumption of the common technology and SOC system architecture. Then this paper proposes a low-power SOC implementation strategy to meet the requirements of this system.

### The Composition of CMOS Circuit Power Consumption

CMOS circuit power consumption is divided into two parts: dynamic power consumption and static power consumption.

Static power dissipation is the amount of power dissipated by the leakage current in the transistor when the circuit is not inverting and only powered. Mainly refers to the leakage current caused by the power consumption, it has become a leakage power. Leakage current can be divided into the following four parts[1]:The current from Drain through the weak inversion layer to Source(IDS); The current flowing from the gate through the thin gate oxide to the Sub due to the tunneling effect and the hot carrier effect (IGATE); The current from Drain to Sub is caused by the strong electric field at the Drain end(IGIDL); The current from Drain and Source to Sub(IREV). The chip's static power consumption is the sum of the power dissipation caused by the total leakage current. It can be expressed as[1]:

$$P_{leakage} = V_{dd} * (IDS + IGATE + IGIDL + IREV) \tag{1}$$

Dynamic power dissipation is the energy consumed by the circuit when it is turned over. It is divided into switching power consumption and short circuit power consumption[3,4].In general, short-circuit power consumption can generally be ignored. The use of 55nm process of this SOC, in this process under static power consumption is relatively large.

### The Common SOC low-power design methods

At present, the industry commonly used low-power technology: Clock-Gating, Multi-threshold libraries, etc.. Newer technologies are Multi-Voltage, MTCMOS Power Gating, Dynamic Voltage and Frequency Scaling, Low-Vdd Standby and so on.

The dynamic power consumption can be reduced by reducing the operating voltage, reducing the inverting load, and reducing the circuit rollover rate. As the most commonly used method to reduce dynamic power consumption, the basic idea of clock shutdown is in the register does not work, turn off the clock, so the buffer and the registers on the clock tree will no longer have dynamic power consumption.

The static power consumption can be reduced by reducing the operating voltage and reducing the leakage current. Reduce the static power consumption of the most intuitive and effective idea is to turn off its power when the circuit is not in work, so that no static power on the whole. When the need for circuit work, then turn on the power, this is the power-down technology. You can choose to disconnect VDD or disconnect VSS for Power-Gating.

### The SOC architecture and low power strategy

The architecture of SOC is shown in Figure 2. The SOC includes four on-chip CPUs, and the internal communication interface processing module (such as CAN, FMAC, UART, etc.) can be connected with other communication systems through the interface chip on the system. SOC on-chip CPU and part of the interface module in the absence of communication is turned off to save power.

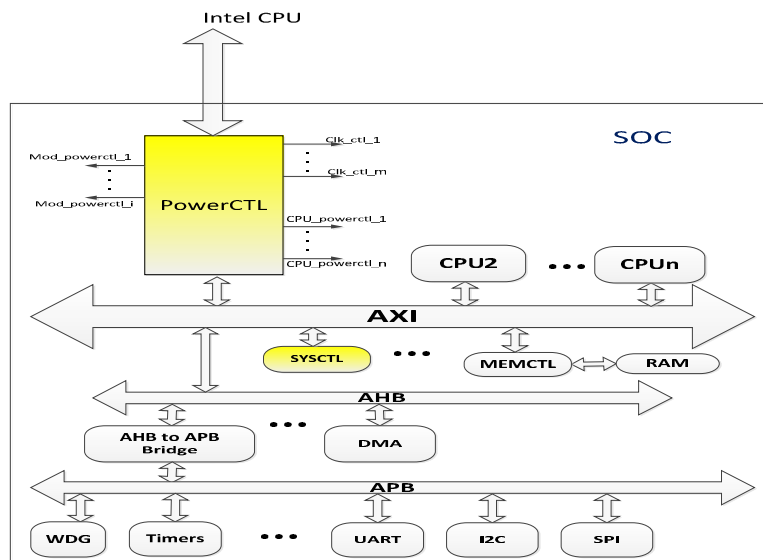


Fig.2. SOC Architecture with Power Controller

The low-power implementation of the SOC requires both reduced dynamic and static power consumption. A low power implementation strategy is presented below. Designed to achieve the clock off and power off the control circuit used in SOC internal. So as to realize the flexible control of the SOC and reduce the dynamic and static power consumption.

According to the operating requirements of the communication system, SOC operating mode can be divided into full-speed mode, low-power mode of operation, deep sleep mode:

(1) full-speed mode: That is, all on-chip CPU and functional modules in the normal working mode. At this point the peak power consumption.

(2) low-power mode of operation: Only the on-chip CPU and modules required by the service are operating normally. Other CPUs and modules that do not need to be operated temporarily are in the power or clock off state.

(3) deep sleep mode: In addition to PowerCTL, SYSCTL, and MEMCTL modules, all other modules with low-power control are placed in the shutdown state. This mode achieves the lowest SOC energy consumption. Such as all on-chip CPUs, UART, etc. are turned off the power. CAN,

FMAC, etc. are turned off the clock. An external Intel CPU is required to wake the SOC from Deep-sleep mode.

According to the system application requirements and the use of digital IP, this SOC implements four low-power methods: Clock-Gating, Multi-threshold libraries; Multi-Voltage, Power-Gating. As shown below:

(1) Multi-Voltage. For CPUs, bus, DMA and other high-speed operation modules, the operating voltage is 1.2V. For SPI, UART, CAN and other low-speed modules, the operating voltage is 1.0V.

(2) Multi-threshold libraries. For high-speed modules, a low-threshold device library is used in the back-end design, with faster inversion and higher power consumption. For low-speed modules, the back-end design is mapped to a high-threshold device library, and reduce the power consumption of its run-time.

(3) Clock-Gating. Some of the modules used in this chip( such as CAN) can be awakened by data transmission on the network after the clock is turned off. So the low-power implementation of these modules is to take the clock off.

(4) Power-Gating. The way to minimize the static power consumption of other modules(such as CPUs, SPI, etc.) is to turn off their power.

For the realization of Multi-Voltage, the back-end design based on the front-end code and UPF file to complete the planning of the implementation of multi-voltage domain. Multi-threshold libraries is also completed by the back-end designing. In this low-power strategy the on-chip CPUs and the off-chip Intel CPU can control the clock and power switch, by controlling the PowerCTL module output the corresponding clock power switch control signals. In order to maintain the versatility and portability of the PowerCTL module, it only responds to the read and write operations of the CPUs and outputs the clock and the power control signals.

The SYSCTL module cooperates with PowerCTL to complete the SOC low power control. It outputs the clock and reset signals to the on-chip CPUs and other modules. When the PowerCTL module issues a clock shutdown signal, SYSCTL turns the corresponding output clock off. SYSCTL automatically initiates a soft reset of the wake-up on-chip CPU when the power to the CPU is turned off and then turned on, that allowing the CPU to re-run from the software's start address.

PowerCTL is the core control circuit of this low power strategy. The design implementation is described in detail below.

### **Design of PowerCTL for Low-Power Control**

The master-slave control requirements of the system require that the PowerCTL have a higher priority than the on-chip CPUs for receiving control information from the off-chip Intel CPU. The PowerCTL module is connected to the AXI bus of the SOC. Its structure as shown in Figure 3.

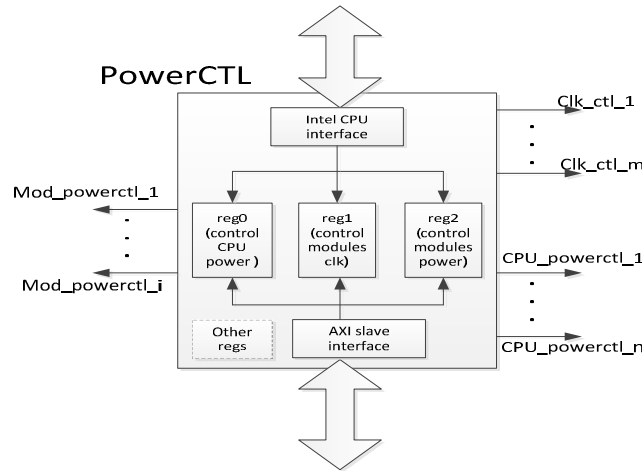


Fig.3. The structure of low-power controller

PowerCTL has an AXI slave interface that supports read and write operations. It can receive the configuration information sent by each CPU on-chip through the AXI bus (according to the standard AXI protocol). The AXI slave interface Receive and parse the information from the bus, resolve the chip-select, write-enable and offset- address signals and then configure the internal three low-power output control register ( reg0, reg1, reg2). PowerCTL also includes a CPU interface in Intel mode to support read and write operations. It can receive the configuration information that the Inter CPU outside the chip passes through the interface.

The PowerCTL contains three control registers: reg0, reg1, reg2 with offset addresses 0, 1, and 2, respectively. The PowerCTL send output clock and power control-signals are controlled by these three registers and are active-high. The bit widths of the three registers are all configurable. The default registers' values after reset is all 0s (that means the default output clock, the power-down signal is inactive). These three registers can receive read and write control from the off-chip CPU and the AXI bus interface. Other registers within the PowerCTL can cache additional information between on-chip CPUs and off-chip CPU.

Three parameter variables are defined inside PowerCTL to keep the bit widths of the set registers and output signals consistent when PowerCTL is instantiated. These three parameter default values:

parameter i = 12; ( This indicates the number of power switches for the internal modules )

parameter m = 4; ( This indicates the number of clock switches for other modules )

parameter n = 4; ( This indicates the number of power switches for the on-chip CPU )

Register reg0 controls the CPU\_powerctl\_1 ... n control signal output to the on-chip CPU power-down. The register reg1 controls the clock off signal clk\_ctl\_1 ... m that is output to the SOC module. Register reg2 controls the power-down signal mod\_powerdown\_1 ... i that is output to the other modules of the SOC. The characteristics of the low-power control signal outputted by the present controller are as follows:

1. When the PowerCTL receives a configuration instruction issued by the Intel CPU or the on-chip CPU to shut down the clock or power of other function modules within the SOC, the corresponding clock or power-down enable signal of the corresponding bit is valid, the clock or power of the corresponding module is shut down. On the contrary, PowerCTL output control clock or power-off signal is invalid, can open the corresponding module clock or power switch.

2. When the PowerCTL receives an instruction from the Intel CPU to power down or power-on the on-chip CPU, the PowerCTL can control the corresponding CPU power-down / on.

3. When the PowerCTL receives the instructions from the on-chip CPU to turn off /on the power

of other on-chip CPUs, the PowerCTL will set the power-down control signals to be valid/invalid.

4. When PowerCTL receives the configuration information sent by Intel CPU and on-chip CPU at the same time, the priority of Intel CPU is higher. When the Intel CPU and the on-chip CPU each control the low-power control signals of different modules, the PowerCTL module responds independently to the configuration information from the on-chip and off-chip CPUs.

5. PowerCTL modules can be configured independently for each on-chip CPU. The output of the controller remains in the most recently configured state.

6. When all on-chip CPUs are powered down, the PowerCTL module is configured by the Intel CPU to determine whether the low power control signal of each module of the SOC, including the on-chip CPU, is valid. However, when only one on-chip CPU is configured to power down, the Intel CPU and other on-chip CPUs which not power down can turn the power of that CPU on.

## Conclusions

By analyzing the results of post-simulation of SOC, the on-chip CPU and function modules can enter/exit the low-power state flexibly. After the clock is turned off, the power consumption of CAN module is reduced by 70%. After the power is turned off, the power consumption of UART drops nearly 80%. While the on-chip CPU power down, the power consumption dropped more. This proves that the proportion of static power consumption is large under 55nm process. Low power control highlights its effectiveness.

The design of the master-slave low-power consumption control circuit not only can control the on-chip CPU power switch, but also can control the power switch or clock switch of each function module in SOC chip by the off-chip CPU. This reduces the on-chip CPUs' load and increases the on-chip CPUs' speed. This not only reduces the power consumption of SOC, and on-chip and off-chip software can flexibly control the clock and power switch. This achieves a balance between functional implementation and low power consumption. Low-power design throughout the SOC design at all levels. With the deepening of research, low-power technology will be more mature. Its flexibility and effectiveness will be greatly enhanced.

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