Advances in Computer Science Research, volume 63
International Conference on Artificial Intelligence and Engineering Applications (AIEA 2016)

Study of Integrated LDO on Chip

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Abstract. In this paper, we first analyze the structure of LDO and analyze its key parts. Secondly, it analyzes the important parameters of LDO, which is helpful to finish the design better. Finally, we pay attention to the particularity of LDO, LDO design, simulation results to meet the design requirements. This circuit has been realized by 0.35μm CMOS process. This LDO exhibits high performance.

Keywords: LDO; SoC; integrated.

1. Introduction

Modern electronic equipment cannot be separated from the power supply circuit, the power circuit performance is good or bad, often determines the life and performance of electronic equipment. Power management chip will be a variety of external power supply after the transformation, to provide a stable and reliable power supply for electronic equipment. In addition to the basic requirements of stable and reliable, modern electronic equipment put forward more requirements, such as the power chip: high efficiency, fast response, low noise, high power density, high PSRR, safety protection and so on.

Power management chip is a kind of different voltage between the bridge and the conversion chip. In an electronic system, the analog circuit and digital circuit, due to the different processes, power, and so on, generally requires a different set of power supply voltage, so the role of power management chip is very important[1~2].

In the application of electrical products, the transformation of the power supply includes: (1) AC/DC; (2) DC/AC; (3) AC/AC;(4) DC/DC.

There are three kinds of power management mode can change one kind of DC voltage to another: (1) LDO linear regulator for Buck converter; (2) Pump Charge type voltage converter; (3)Inductive switch type DC-DC converter.

2. Structure of LDO

LDO is divided into conventional and on-chip integrated LDO two categories, the conventional LDO need to add a 0.1-10uF output filter capacitor, the capacitor used to absorb the transient transition during the output voltage overshoot and undershoot, while Also ensure LDO stability. However, 0.1-10uF filter capacitor cannot be achieved on-chip integration, only through the chip pad connected to the printed circuit board on-chip capacitors to achieve, but the chip pad will take up a lot of area, while the chip pad to the chip pin Of the connection line will introduce parasitic inductance and parasitic resistance, affecting chip performance, another 0.1-10uF chip capacitors will increase the system cost. In response to these shortcomings, on-chip integrated LDO was proposed. The on-chip integrated LDO output capacitor ranges from 0 to 100 pF. On-chip LDOs can be individually powered for each circuit module for individual SoC system features, while on-chip LDOs can be placed near power-fed circuit blocks to provide the required voltage accuracy, power supply capability, power supply rejection Noise, transient response, etc. [3], to improve the overall performance of the system. The on-chip integrated LDOs are simple in structure and can be fully integrated inside the chip and placed next to the powered circuit blocks while eliminating external on-chip capacitors, saving chip pad and associated pin area and speeding up the manufacturing process.

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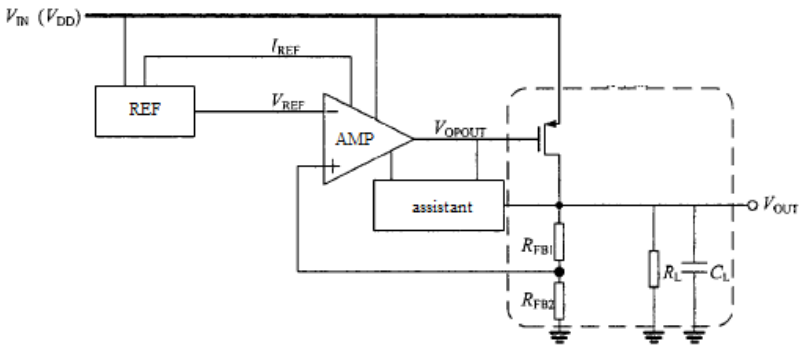

Fig. 1 Structure of LDO

LDO is a typical application of the operational amplifier and the closed loop negative feedback system, which can be used to achieve the stable output voltage under different output current. Fig.1 shows the typical structure and basic composition of LDO. LDO is composed of four modules, which are the most basic modules, respectively: (1) reference circuit; (2) error amplifier; (3) power level; (4) auxiliary circuit.

Power level off chip load resistance and load capacitance are also included in this is because the two devices have a significant impact on the frequency response of the LDO and the changes in the operating point.

The output voltage of LDO can be expressed as:

$$V_{OUT} = V_{REF} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \left(1 - \frac{1}{1 + \frac{R_{FB2}}{(R_{FB1} + R_{FB2}) \cdot A_{O,EA} \cdot AO, POW}} \right) \tag{1}$$

The reference voltage circuit can provide a stable reference voltage (Uref). Commonly used voltage reference source structure is Zener diode or bandgap reference source, which is generally used for the former supply voltage greater than 7V and the temperature change is not demanding system And the bandgap reference source is suitable for low-voltage and high-precision power supply system. Adjusted tube is also called power tube, the main role is as input to the output of the high current channel, and has a certain input and output voltage difference and output current NPN, PNP, NMOS and PMOS. The feedback network is usually composed of resistor networks, the main role is to feedback the output voltage to the error amplifier input, that is, to adjust the output voltage, the error amplifier, regulator and feedback network form a closed-loop feedback system [4].

The output voltage of the LDO is only dependent on the reference voltage and the feedback factor, independent of the input voltage. So in a given reference voltage can be adjusted by adjusting the feedback coefficient to determine the output voltage. The relative accuracy of the integrated resistors in the integrated circuit fabrication process is very high and a very accurate feedback coefficient can be easily obtained.

3. LDO Key Indicators

LDO key indicators include the voltage drop, load regulation, linear regulation, and quiescent current and transient response. In the LDO design, these indicators are mutually influential, and there is a compromise between the indicators. In order to optimize the performance of LDO, we must first analyze the relationship between these indicators, through innovative design to break the trade-off between them to achieve low power ultra-fast response LDO [5, 6].

(1) Dropout Voltage

Dropout Voltage is one of the most important design specifications of an LDO, defined as the difference between the supply voltage and the output voltage at which the output voltage of the LDO will no longer be regulated to the desired value when the supply voltage drops to a certain value.

LDO works properly when working with regulation region. The output voltage Vout of the LDO is normally regulated by the loop, and the output voltage Vout is little affected by the supply voltage

Vdd. As the power supply voltage decreases, the output voltage Vout of the LDO is determined by the supply voltage VDD, as the power supply voltage VDD drops, the output voltage Vout approaches a constant amplitude drop, whereupon the LDO enters the Dropout region. When the supply voltage VDD continues to drop, the LDO will be in the off region, and the output voltage Vout drops to near ground potential. Industry-wide differential voltage measurement standard is the output voltage dropped to 98% of the standard value, the power supply voltage VDD and the difference between the output voltages Vout.

(2) Load Regulation

It is used to measure the LDO's ability to stabilize the Vout when the load changes.

(3) Line Regulation

It is used to measure the LDO's ability to stabilize the Vout when the supply voltage changes.

(4) Quiescent Current

LDO quiescent current refers to the LDO power supply current and load current difference between, that is, in addition to LDO power flow through the MP tube all the current outside the current.

The quiescent current of the LDO includes the operational amplifier bias current, the quiescent current of the bandgap reference, and the protection circuit and output buffer stage currents.

If the LDO is used in a battery-powered mobile system, the quiescent current at the lowest load current is important. When the load current increases or in some low power consumption requirements of applications, LDO quiescent current can be increased, thereby enhancing the transient performance of LDO.

(5) Transient response

LDO's transient response is usually composed of load transient response and linear transient response, it directly affects the performance of the LDO circuit, because of the load conditions will change at any time, and the load transient response is the most important LDO Of the parameters of one of the indicators. Generally speaking, the digital circuit anti-interference ability, the power supply voltage tolerance higher, and analog circuits and RF circuits require power supply voltage stability, power supply voltage disturbance over the General Assembly affect the normal work of the circuit. Load Transient Response From load transients, the overshoot and undershoot of the output voltage are determined at settling time. In practice, the load current switching time, IL change, the power transistor Mp gate slew rate, LDO Gain Bandwidth Product GBW, Phase Margin and output capacitance and other factors.

4. Circuit Design

The goal of the power management system on the SOC is to achieve lower power supply noise. The main sources of power supply noise are power supply noise, power supply noise itself, as well as shared power supply system, the noise generated by other modules. Reduce the external power supply noise interference is actually to improve the power supply module power supply rejection ratio performance; and reduce the noise of the power supply itself is to design low output noise of the power supply; and for the common power line noise can be generated by a certain power Management strategy to suppress.

In the design of the LDO group needs to consider the comprehensive compromise factors: area, loop gain, transient response and stability.

Loop gain is conducive to improving the system's linear regulation and load regulation performance. However, gain and bandwidth are often contradictory. Increasing the gain usually results in lower system bandwidth, which means that the transient performance of the LDO is degraded. Increase the loop gain methods are: increase the gain level, increase the bias current, increase the output impedance, and increase the size of the conduction tube.

Increasing the gain stage will likely introduce low-frequency poles, affecting the stability of the system. Increasing the bias current will increase the quiescent current of the system, that is, increase

the power consumption of the system. At the same time, the output impedance of the amplifier may increase and the parasitic pole will be low, which will affect the system stability. Increasing the output impedance will reduce the output pole frequency, thereby degrading the stability of the system. Increasing the size of the conducting pipe will cause the gate capacitance of the adjusting transistor to increase and the load transient response of the LDO will become slower and worse. Also, the above-described increase in gain stage and increase in the size of the conduction pipe also leads to an increase in the area of the chip and an increase in the cost of the system.

The choice of output capacitor is also true. Selecting a large load capacitance improves load transient response, but increases the area and cost of the system. In addition, the choice of a different capacitor needs to reconsider the stability of the loop.

This circuit has been realized by 0.35μm CMOS process. This LDO exhibits high performance. The design of the on-chip LDO is shown in Fig.2.

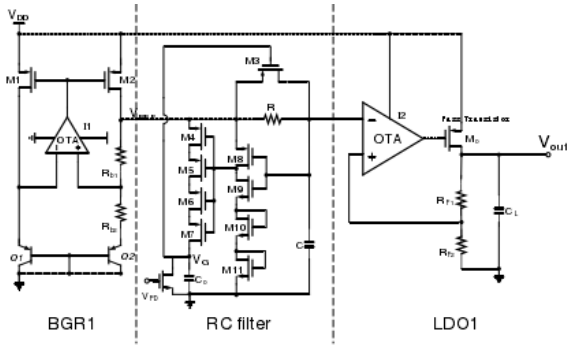

Figure 2. The design of the LDO circuit

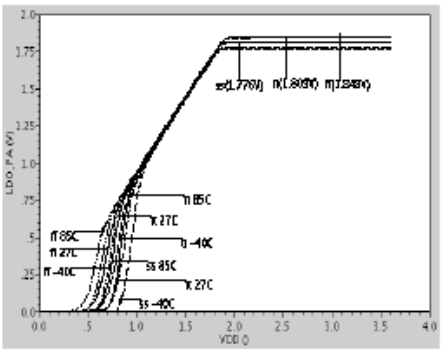

Figure 3. The output voltage of LDO

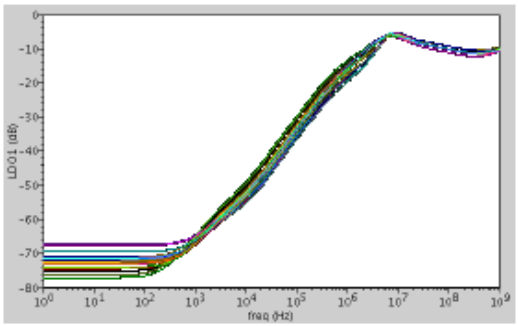

Figure 4. PSRR of LDO

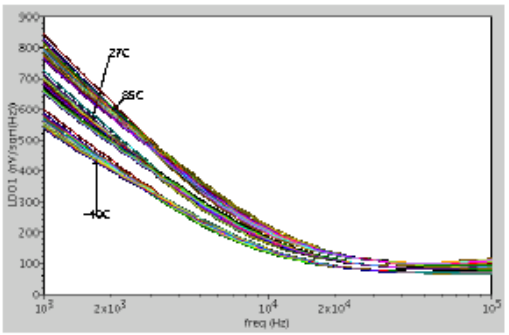

Figure 5. Output noise of LDO

Figure 3 to Figure 5 is on-chip LDO simulation curve. From the simulation curve can be seen, LDO to meet the requirements of on-chip power supply.

5. Conclusion

In this paper, we first analyze the structure of LDO and analyze its key parts. Secondly, it analyzes the important parameters of LDO, which is helpful to finish the design better. Finally, we pay attention to the particularity of LDO, LDO design, simulation results to meet the design requirements.

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