Soft-switching dual full-bridge converter with reduced circulating loss and voltage stress of secondary rectifier

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Abstract. This paper proposes a novel soft-switching dual full-bridge converter with shared lagging leg and dual outputs in series. Resonant clamp circuits are employed across the secondary rectifiers to reduce the voltage overshoots of the secondary rectifiers, as well as extinguish the primary current during the freewheeling interval. Full Zero-Voltage-Switching (ZVS) range of the lagging leg switches can be achieved based on the parallel full-bridge configuration. The dual outputs of the proposed converter are connected in series, and the whole output voltage can be regulated within the desired voltage range by the phase-shift control. Therefore, the proposed converter would be useful for high output voltage and high power applications. Steady state operation and distinctive features of the converter are explained and verified on a 1-kW hardware prototype, and experimental results validate the feasibility and performance of the proposed converter.

Keywords: dual full-bridge; ZVS; phase-shift control; shared lagging leg; high output voltage.

1 Introduction

In recent years, the conventional phase-shift full-bridge (PSFB) converters have been widely employed in high-power applications [1-5] because of their advantages of high conversion efficiency, high power density, and low electromagnetic interference (EMI). All primary switches can be turned on under ZVS using the transformer leakage inductance and switch intrinsic capacitance without any external passive components [6-9]. It is well known that the energy stored in the output inductor is sufficient to help the leading leg switches realize ZVS for a wide load range. But it is difficult to realize ZVS for the lagging leg switches under light load conditions because the energy stored in the small leakage inductance is always insufficient especially under high input voltage and light load conditions. The ZVS range can be extended by increasing the leakage inductance and/or adding a suitable series inductance. However, having a large series inductance reduces the effective duty ratio and limits the power transfer capability of the converter. Moreover, some other problems are brought in, such as high voltage spikes on the secondary-side rectifiers, excessive primary circulating current [10-15], etc. Therefore, several methods [16-22] have been proposed to solve these problems with the conventional PSFB converters.

Recently, several hybrid Half-bridge Full-bridge (HB-FB) converters based on “shared leg” technique have been proposed in [23-28]. Their common characteristic is that the input energy can be

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transferred to the output even in the freewheeling interval of the output inductor. In this way, The requirements for filter are less because of the three-level voltage waveforms of the secondary-side rectifier, and the efficiency can be significantly increased because of the parallel power processing technique [29]. The hybrid HB-FB converter in [23] employs an additional transformer, which is connected between the mid-point of the split capacitor to the mid-point of the lagging leg, to realize fully ZVS of the lagging leg switches. However, when the primary-side of the main transformer is shorted in the freewheeling interval, a circulating current will be created due to series connection of the secondary sides of the two transformers, resulting in severe conduction loss. In [24], the two split capacitors are replaced with two active switches, and the performance of the proposed converter is analyzed for constant-input, variable-output applications. Nevertheless, the circulating current problem still exists. The topology in [25] replaces the additional transformer with two active switches. In this way, the board space can be saved and the power density will be increased. The circuit configuration can be changed from full-bridge to half-bridge during the freewheeling interval. The input energy is transmitted to the output load with no dead time, and therefore the input current ripple and output filter requirement can be greatly reduced. However, its main disadvantage is that ZVS capability of the lagging leg switches will be lost at light loads. Loss of ZVS implies high switching losses at high switching frequency and may also result in possible reliability problems such as device failure due to poor reverse recovery characteristic of the MOSFET body diode.

In order to solve this problem, a Zero-Voltage Zero-Current-Switching (ZVZCS) hybrid HB-FB converter has been proposed in [26] for high input voltage application. The leading leg employing MOSFETs is a three-level (TL) leg, where the active switches can realize ZVS for a wide load range and suffer only half of the input voltage. The lagging leg adopting IGBTs is a two-level leg, and operates at ZCS in the full-load and full-line range. However, the conduction loss in the two-level leg increases and the magnetizing energy of the transformer can not be fed back to the input because of the series diodes. Moreover, utilization of the input voltage is relatively low due to the primary blocking capacitor [27].

Recently, attention has been drawn to hybrid resonant and PWM converters [27, 28]. A soft-switching converter combining the LLC resonant half-bridge circuit and PSFB circuit with a shared ZVS leading leg has been proposed in [27]. In this converter, full ZVS range of MOSFETs in the leading leg is realized based on the parallel LLC resonant half-bridge configuration. The primary current is extinguished by the output voltage of LLC resonant circuit during the freewheeling interval. ZCS of IGBTs in the lagging leg can be achieved in the complete full-line and full-load range. Furthermore, duty cycle loss is negligible since the leakage inductance of the main transformer can be designed as small as possible. However, this way also results in high voltage spikes on the secondary side rectifiers because of the lack of clamping feature. In consequence, this will increase the voltage stress across the rectifiers and may result in EMI problems. Also, a novel high-efficiency hybrid HB-FB converter with shared lagging leg is developed in [28]. In this topology, ZVS of the active switches in the lagging leg can be realized from true zero-load to full-load condition with the help of LLC resonant circuit. The secondary-side resonant circuit can quickly reset the primary circulating current during the freewheeling interval, as well as reduce voltage overshoots across the rectifier diodes and transfer additional resonant energy to the output load. Hence, the proposed converter is attractive for hybrid electric vehicles (HEVs)/electric vehicles (EVs) on-board charger applications.

This paper proposes a novel dual full-bridge converter with shared lagging leg and dual outputs in series. In this converter scheme, ZVS of the active switches in the lagging leg can be realized for full power range based on the parallel full-bridge configuration. Resonant clamp circuits are employed across the secondary rectifiers to reduce the voltage overshoots of the secondary rectifiers, as well as extinguish the primary current during the freewheeling interval. It is also known that, the voltage stresses on the output stresses on the output terminal power devices can be reduced because of the dual outputs in series configuration. In consequence, rectifiers with lower breakdown voltage rate, better reverse recovery characteristic and lower forward voltage drop can be used, and this can reduce conduction loss and reverse recovery loss of the secondary rectifier. Hence, there is a lot of potential for this converter to be used for high voltage and high power applications.

This paper is organized as follows: Section II describes the circuit configuration and detailed operation principle of the power stage. Some detailed features and characteristics are analyzed in Section III. In Section IV, a 1-kW hardware converter prototype has been designed, made and tested to verify the validity and superior performance of the proposed circuit. Finally, the concluding remarks are presented in Section V.

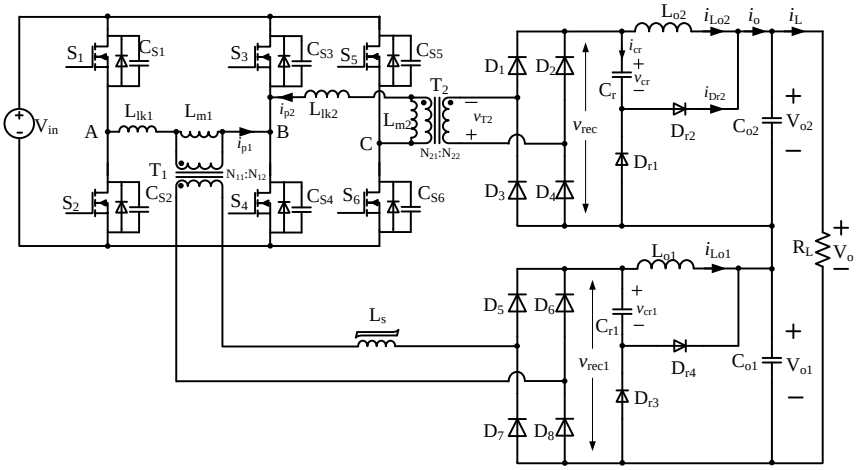

Figure 1. Circuit configuration for the proposed converter

2 Operation and analysis

Fig. 1 shows the circuit diagram of the proposed converter which composed of two parts. The first part is a uncontrolled full-bridge (FB1) circuit, including four MOSFETs S_1-S_4, a tightly coupled transformer T_1 with an air gap, a saturable inductor L_s, a secondary-side rectifier (D_5-D_8), a resonant clamp circuit Aux1 (C_{r1}, D_{r3} and D_{r4}), and a LC output filter (L_{o1} and C_{o1}). The second part is a phase-shift full-bridge (FB2) circuit, including two MOSFETs S_3 and S_4 as lagging leg, two MOSFETs S_5 and S_6 as leading leg, a tightly coupled transformer T_2, a secondary rectifiers (D_1-D_4), a resonant clamp circuit Aux (C_r, D_{r1} and D_{r2}), and a LC output filter (L_{o2} and C_{o2}). The operation principle of the proposed converter can be briefly explained as follows: the FB1 is uncontrolled and the diagonal pair of switches conducts together, hence the output voltage (V_{o1}) of the FB1 circuit is at its maximum value and the whole output voltage (V_o) is regulated by the FB2 circuit with phase-shift control. The resonant clamp circuit Aux extinguishes the primary current in the transformer T_2 during the freewheeling interval by imposing the voltage across C_r across the transformer secondary. Meanwhile, there is no corresponding freewheeling interval in FB1 circuit operation, and therefore the resonant circuit Aux1 is used just to clamp secondary rectifier voltage.

In the active interval, the leakage inductance L_{lk2} of the transformer T_2 resonates with C_r. The resonant frequency is given by

$$\begin{cases} f_r = \dfrac{1}{2k_2\pi\sqrt{L_{lk2}C_r}} \\ T_r = 1/f_r \end{cases} \tag{1}$$

where k_2 denotes the turns ratio N_{22}:N_{21} of the transformer T_2. T_{on} is the active interval when the diagonal pair of switches (S_3, S_6) or (S_4, S_5) conduct together, and T_s is the switching period, then we can derive D=2T_{on}/T_s as the duty cycle of the FB2 circuit. According to the relationship between T_{on} and T_r as shown in Table I, there are three distinct operation modes for the proposed converter [28]. In Mode 1 operation, the FB2 circuit still works in the active interval when the resonant current i_{Dr2} reaches zero. In Mode 2 operation, the FB2 circuit turns into the freewheeling interval just at the

instant when the resonant current i_{Dr2} reaches zero. In Mode 3 operation, the FB2 circuit turns into the freewheeling interval before the resonant current i_{Dr2} reaches zero.

Table 1. Mode Selection Criteria

Mode 1	Mode 2	Mode 3
$T_{on}>T_r/2$	$T_{on}=T_r/2$	$T_{on}<T_r/2$

2.1 Mode 1

The proposed converter goes through nine stages during a half-switching cycle in this mode. The equivalent operation circuits and key waveforms for different stages are shown in Figs. 2 and 3, respectively.

Switches S_2, S_3 and S_5 conduct prior to Stage 1 and the primary current i_{p2} in the transformer T_2 is reset because of the resonant clamp circuit Aux. Meanwhile, the magnetizing current of TR2 is negligible since the magnetizing inductance L_{m2} is designed to be large. Also, the saturable inductance value is zero since the secondary current of transformer T_1 is larger than the critical saturation point.

Stage 1 [$t_0 \le t < t_1$]: At $t=t_0$, S_2 and S_3 are turned off. The primary current i_{p1} charges the output capacitors of S_2 and S_3 and discharges that of S_1 and S_4. The voltage across switch S_3 can be expressed as

$$v_{s3}(t)=\frac{k_1 i_{Lo1}+I_{Lm1}}{2C_{so}}(t-t_0) \tag{2}$$

where v_{s3} is the voltage across switch S_3, k_1 denotes the turns ratio N_{12}:N_{11} of transformer T_1, i_{Lo1} is the output inductor current, I_{Lm1} is peak value of the magnetizing current i_{Lm1}, and I_{Lm1} is given by

$$I_{Lm1}=\frac{V_{in}}{2(L_{m1}+L_{lk1})}\frac{T_s}{2} \tag{3}$$

where V_{in} is the input voltage, L_{m1} and L_{lk1} are the magnetizing inductance and leakage inductance of transformer T_1, respectively.

Stage 2 [$t_1 \le t < t_2$]: During Stage 2, the voltage difference between the voltage v_{s3} and the reflected voltage (v_{cr}/k_2) is applied to the leakage inductance L_{lk2} of transformer T_2, and the primary current i_{p2} can be expressed as

$$v_{s3}-\frac{v_{cr}}{k_2}=L_{lk2}\frac{di_{p2}}{dt} \tag{4}$$

where L_{lk2} is the leakage inductance of transformer T_2. During this interval, the primary current i_{p1} continues to charge the output capacitors of S_2 and S_3 and discharge that of S_1 and S_4.

Stage 3 [$t_2 \le t < t_3$]: During this stage, the primary current i_{p1} decreases quickly to the magnetizing current i_{Lm1} since the leakage inductance L_{lk1} is designed to be very small. The saturable inductor L_s turns into a high impedance state, and therefore the primary-side and secondary-side power circuits of FB1 are separated. Also, i_{Lm1} can be assumed constant and at its peak value I_{Lm1} during this interval. The diode D_{r3} conducts and the inductor current i_{Lo1} flows through C_{r1}, D_{r3} and L_{o1} for freewheeling. During this interval, the output capacitor of S_2 is charged by I_{Lm1}, whereas that of S_3 is charged by the difference current between I_{Lm1} and i_{p2}. The voltages across S_2 and S_4 are expressed respectively as

$$\begin{cases}\dfrac{I_{Lm1}}{2}=C_{so}\dfrac{dv_{s2}}{dt}\\[2ex] \dfrac{I_{Lm1}-i_{p2}}{2}=C_{so}\dfrac{dv_{s3}}{dt}\end{cases} \tag{5}$$

where v_{s2} is the voltage across switch S_2. As indicated in (5), it should be noted that it is more difficult for S_3 to realize ZVS comparing with S_2 because of the different charging current. According to equations (4) and (5), the current i_{p2} and voltage v_{s3} can be calculated as

$$\begin{cases} i_{p2}(t) = I_{Lm1} - \left[I_{Lm1} - i_{p2}(t_2)\right]\cos\left[\omega_0(t-t_2)\right] + \dfrac{\left(V_{in}/2 - v_{cr}/k_2\right)}{Z_0}\sin\left[\omega_0(t-t_2)\right] \\ v_{s3}(t) = \dfrac{v_{cr}}{k_2} + \left(\dfrac{V_{in}}{2} - \dfrac{v_{cr}}{k_2}\right)\cos\left[\omega_0(t-t_2)\right] + Z_0\left[I_{Lm1} - i_{p2}(t_2)\right]\sin\left[\omega_0(t-t_2)\right] \end{cases} \tag{6}$$

where $Z_0 = \sqrt{2C_{so}/L_{lk2}}$ and $\omega_0 = 1/\sqrt{2L_{lk2}C_{so}}$, $i_{p2}(t_2)$ is the primary current of T_2 at t_2. The body diode of S_4 begins to conduct when the output capacitor of S_3 is charged to the input voltage V_{in}.

Stage 4 [$t_3 \le t < t_4$]: At t=t_3, switches S_1 and S_4 are turned on with ZVS. The saturable inductance value turns into zero quickly and the leakage inductance L_{lk1} resonates with the lumped secondary capacitance. Meanwhile, the secondary rectifier voltage v_{rec1} increases rapidly to the value of (v_{cr1} + V_{o1}), and therefore the diodes D_6, D_7 and D_{r4} conduct to clamp the rectifier voltage. The primary current i_{p2} continues to increase since the voltage difference between the input voltage V_{in} and the reflected capacitor voltage (v_{cr}/k_2) is applied to the leakage inductance L_{lk2}.

Stage 5 [$t_4 \le t < t_5$]: At t_4, D_{r2} begins to conduct and D_{r4} has turned off. The primary current i_{p2} increases beyond the value of ($k_2 i_{Lo2}$) because of the resonance between L_{lk2} and C_r. During this stage, the rectifier voltage v_{rec} is clamped to (v_{cr} + V_{o2}) and the output inductor i_{Lo2} increases nonlinearly.

Stage 6 [$t_5 \le t < t_6$]: At t_5, the FB2 circuit turns into a typical power transfer mode when a diagonal pair of the active switches (S_4 and S_5) is on, and the voltage v_{rec} across the rectifier returns to $n_2 V_{in}$. Stage 6 ends when S_5 is turned off.

Stage 7 [$t_6 \le t < t_7$]: At t=t_6, S_5 has been turned off. During this stage, the primary current i_{p2} charges the output capacitor of S_5 and discharges that of S_6. The switch voltages across S_5 and S_6 can be expressed as

$$\begin{cases} v_{s5}(t) = \dfrac{i_{p2}}{2C_{so}}(t-t_6) = \dfrac{k_2 i_{Lo2}}{2C_{so}}(t-t_6) \\ v_{s6}(t) = V_{in} - v_{s5} \end{cases} \tag{7}$$

where v_{s5} and v_{s6} are the voltages across the active switch S_5 and S_6, respectively. Stage 7 will end once the rectifier voltage v_{rec} deceases to the resonant capacitor voltage v_{cr}. The time t_7 can be obtained by solving (7) and t_7 will be

$$t_7 = t_6 + \Delta t_{6,7} = t_6 + \frac{2C_{so}\left(V_{in} - \dfrac{v_{cr}}{k_2}\right)}{k_2 i_{Lo2}} \tag{8}$$

where $\Delta t_{6,7}$ is the time interval of Stage 7.

Stage 8 [$t_7 \le t < t_8$]: At t=t_7, the diode D_{r1} begins to conduct. During this interval, the voltage difference between v_{s6} and the primary voltage of transformer T_2 is applied to the leakage inductance L_{lk2}. The switch voltage v_{s6} deceases nonlinearly. Therefore, the current i_{p2} and voltage v_{s6} can be expressed as

$$\begin{cases} i_{p2}(t) = k_2 I_{Lo2}\cos\left[\omega_0(t-t_7)\right] \\ v_{s6}(t) = \dfrac{v_{cr}}{k_2} - k_2 i_{Lo2} Z_0 \sin\left[\omega_0(t-t_7)\right] \end{cases} \tag{9}$$

The body diode of switch S_6 begins to conduct after the output capacitor of S_6 has been completely discharged. Then, the time t_8 can be found by solving (9) and t_8 will be

$$t_8 = t_7 + \Delta t_{7,8} = t_7 + \frac{1}{\omega_0}\sin^{-1}\left(\frac{v_{cr}}{k_2}\frac{2C_{so}\omega_0}{k_2 i_{Lo2}}\right) \tag{10}$$

where $\Delta t_{7,8}$ is the time interval of Stage 8.

Stage 9 [$t_8 \le t < t_9$]: During this stage, the primary current i_{p2} of transformer T_2 is reset, and the entire output current is provided by the resonant capacitor C_r. Stage 9 will end once S_1 and S_4 are turned off and the next half switching cycle starts.

2.2 Mode 2

Fig. 4(a) shows the key waveforms of the proposed dual full-bridge converter in Mode 2 operation. The only difference between Figs. 3 and 4(a) is that the proposed converter working in Mode 2 does not have the power conversion process of Stage 6 in Fig 3. This is because the resonant current i_{Dr2} reaches zero exactly at the instant when switch S_5 is turned off.

2.3 Mode 3

The proposed converter goes through eight stages during a half-switching cycle in this mode. The operation of the proposed converter in this mode is almost the same as in Mode 1 except for Stages 6 and 7, and therefore only stages 6 and 7 are discussed in this section. Also, Fig. 5 shows the equivalent operation circuits for Stages 6 and 7 in this mode, and key waveforms for different stages are shown in Fig. 4(b).

Stage 6 [$t_5 \le t < t_6$]: At t_5, S_5 has been turned off. The primary current i_{p2}, which is equivalent to $n_2(i_{Lo2}+i_{Dr2})$, begins to charge the output capacitor of S_5 and that of S_6. During this stage, the output capacitor of S_6 is discharged completely, and then the body diode of S_6 begins to conduct.

Stage 7 [$t_6 \le t < t_7$]: During this stage, the voltage reflected from the secondary-side is applied to the leakage inductance L_{lk2} of transformer T_2 and the primary current i_{p2} continues decreasing. The resonant current i_{Dr2} reaches zero at the end of this stage and the diode D_{r2} turns off.

3 Analysis of the proposed converter

3.1 Transformers Turns Ratios

The input-output relationship of the proposed converter is given below

$$V_o = V_{o1} + V_{o2} = (k_1 + k_2 D)V_{in} \tag{11}$$

where D is the duty cycle of FB2 circuit. This equation shows that the output voltage varies between $k_1 V_{in}$ (when $D = 0$) and $(k_1+k_2)V_{in}$ (when $D = 1$). The turns ratio of the two transformers can be determined according to the range of variation in the input and output voltage. Therefore, k_1 and k_2 can be expressed as

$$\begin{cases} k_1 = \dfrac{V_{o,\min}}{V_{in,\max}} \\ k_2 = \dfrac{V_{o,\max} - k_1 V_{in,\min}}{V_{in,\min}} \end{cases} \tag{12}$$

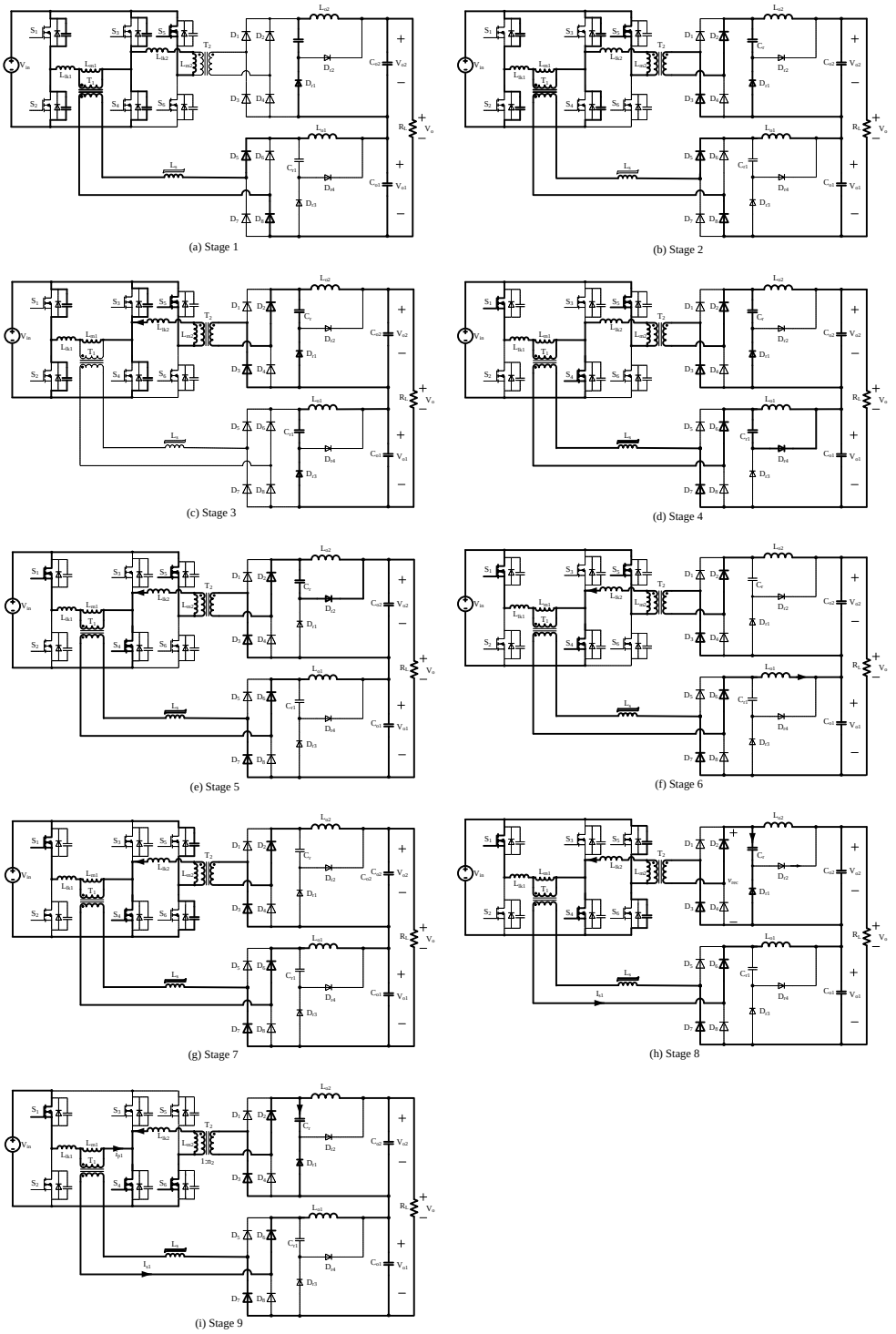

Figure 2. Topological stages of the proposed converter in Mode 1 operation. (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4, (e) Stage 5, (f) Stage 6, (g) Stage 7, (h) Stage 8, (i) Stage 9

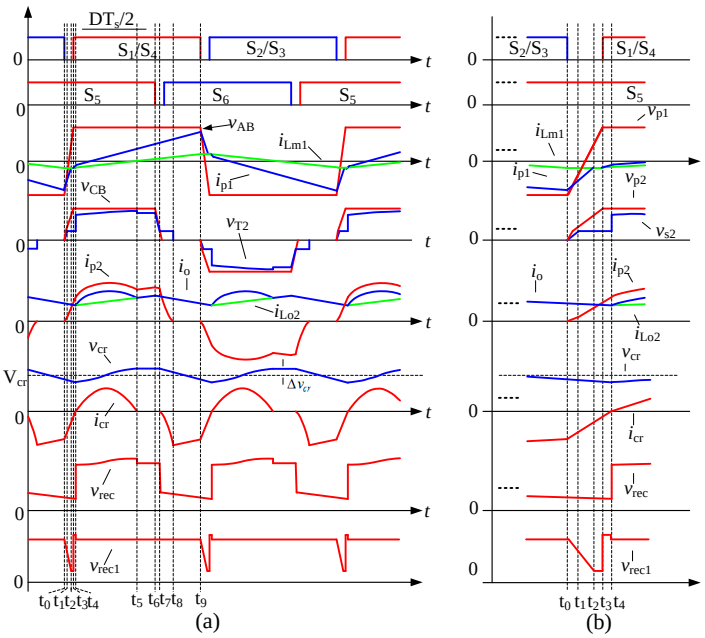

Figure 3. (a) Key waveforms of the proposed converter in Mode 1 operation. (b) enlarged waveforms from t0 to t4

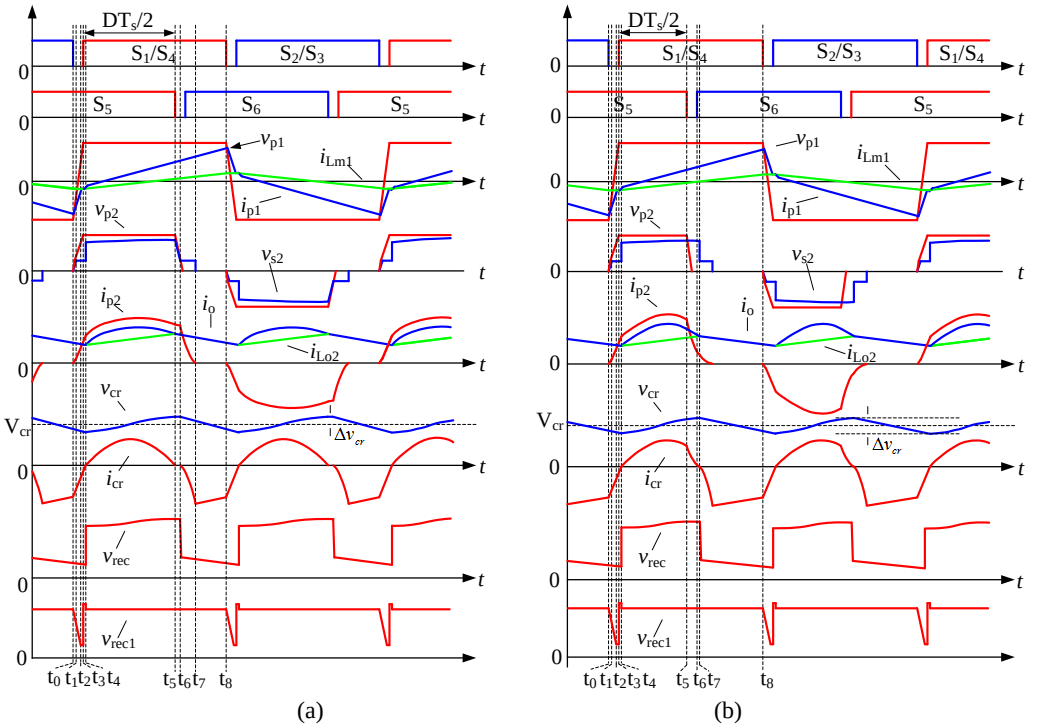

Figure 4. (a) Key waveforms of the proposed converter in Mode 2 operation. (b) Key waveforms of the proposed converter in Mode 3 operation.

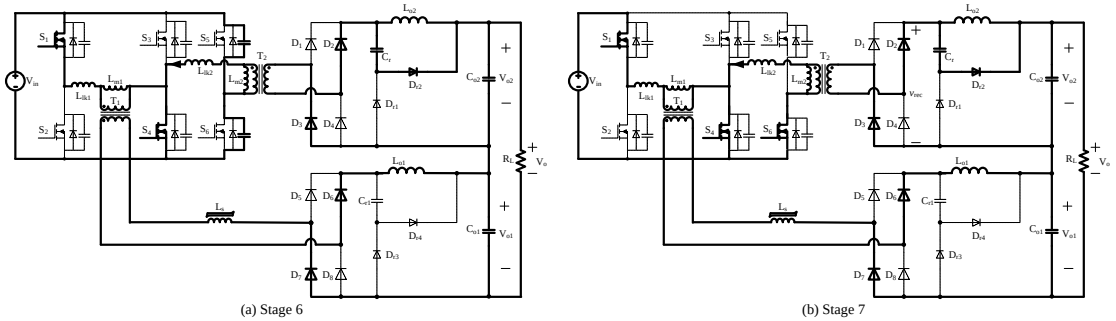

Figure 5. Topological Stages of the proposed converter in Mode 3 operation. (a) stage 6, (b) stage 7.

3.2 Soft-switching conditions for the active switches

The ZVS conditions for the leading leg switches (S_5 and S_6) can be designed in Mode 1 since the primary-side current of FB2 circuit is smaller for the same output power at higher output voltage. Fig.6 illustrates the primary-side current for the conventional PSFB converter and FB2 circuit respectively. In the FB2 circuit, there is no circulating current in the primary-side full-bridge circuits compared to the conventional PSFB converter. As shown in Fig. 6(b), the ZVS conditions for the leading leg switches of FB2 circuit can be expressed as

$$\frac{1}{2}L_{lk2}i_{p2}^2=\frac{1}{2}L_{lk2}\left(k_2 i_{Lo2}\right)^2\geq C_{so}\left(\frac{v_{cr}}{k_2}\right)^2 \tag{13}$$

As indicated in (13), the minimum output inductor current ($i_{Lo2,ZVS}$) to guarantee ZVS of the leading leg switches is given by

$$\begin{cases} i_{Lo2,ZVS}\geq\dfrac{v_{cr}}{k_2^2}\sqrt{\dfrac{C_{so}}{L_{lk2}}} \\ v_{cr}\leq 2\left(k_2V_{in}-V_{o2}\right) \end{cases} \tag{14}$$

In order to ensure ZVS, the dead time $t_{d,\,leading}$, should be adjusted to allow the output capacitors of S_5 and S_6 to fully charge and discharge, and it can be derived as given below based on (8) and (10)

$$t_{d,leading}>\Delta t_{6,7}+\Delta t_{7,8}=\frac{2C_{so}\left(V_{in}-\dfrac{v_{cr}}{k_2}\right)}{k_2 i_{Lo2}}+\frac{1}{\omega_0}\sin^{-1}\left(\frac{v_{cr}}{k_2}\frac{2C_{so}\omega_0}{k_2 i_{Lo2}}\right) \tag{15}$$

In consequence, the ZVS range of the leading leg switches in FB2 circuit can be designed based on (14) and (15). In most operation cases, v_{cr} is relatively small comparing with k_2V_{in} and V_{o2}, and therefore ZVS of S_5 and S_6 can be realized for a wide power range.

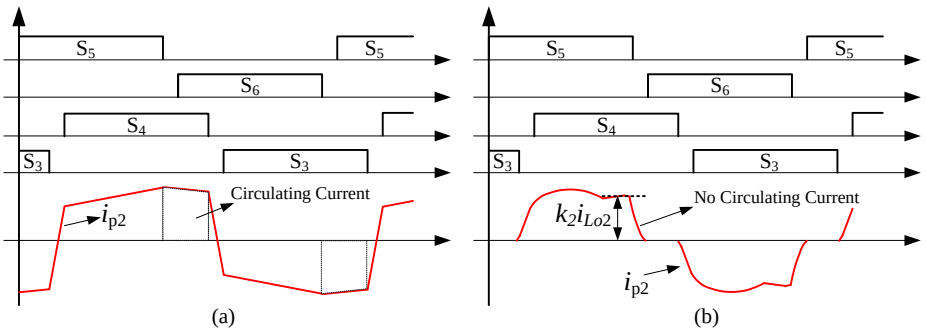

Figure 6. Gate pulses and current waveforms of the primary-side full-bridge circuits: (a) the conventional PSFB converter and (b) FB2 circuit.

As we all known, ZVS of the active switches in the lagging leg is realized relying mainly on the magnetizing current of transformer T_1, and the peak value of magnetizing current i_{Lm1} is independent of load condition. Hence, the ZVS conditions for the primary-side switches of FB1 circuit can be expressed as

$$\frac{1}{2}(L_{m1}+L_{lk1})I_{Lm1}^2 \geq 2C_{so}V_{in}^2 \tag{16}$$

As indicated in (3) and (16), the energy needed to realize ZVS depends only on the magnitude of the input voltage, and is independent of the output voltage. By using (3), the magnetizing inductance L_{m1} is defined as

$$L_{m1} \leq \frac{T_s^2}{64C_{so}} - L_{lk1} \tag{17}$$

In order to ensure ZVS, the dead time $t_{d.lagging}$, should be adjusted to allow the output capacitors of MOSFETs S_1-S_4 to fully charge and discharge under no-load condition, and it is given by

$$t_{d,lagging} \geq \frac{2C_{so}V_{in}}{I_{Lm1}} = \frac{8C_{so}(L_{m1}+L_{lk1})}{T_s} \tag{18}$$

ZVS of S_1-S_4 can be achieved from true zero-load to full-load by selecting of the proper L_{m1} and $t_{d.lagging}$. The selections of L_{m1} and $t_{d.lagging}$ are independent of the input voltage and load condition, as shown in (17) and (18). Thus, ZVS of S_1-S_4 is independent of input voltage variations, the output voltage and output current.

3.3 Reduced voltage stresses of the secondary rectifiers

In the proposed converter, the voltage overshoots arising from the resonance between the leakage inductance and parasitic lumped secondary-side capacitance are significantly reduced by the resonant clamp circuit. For the FB2 circuit, the voltage stresses of secondary-side rectifiers are clamped to

$$v_{rec} = v_{cr} + V_{o2} = V_{cr} + \Delta v_{cr} + V_{o2} \tag{19}$$

where V_{cr} is the average DC voltage and Δv_{cr} is the superimposed rippled voltage across C_r. According to [21], the average DC voltage V_{cr} is given by

$$V_{cr} = k_2 V_{in} - V_{o2} \tag{20}$$

By using (20), the voltage stresses of the secondary-side rectifiers are given by

$$v_{rec} = n_2 V_{in} + \Delta v_{cr} \tag{21}$$

During the freewheeling interval, the resonant capacitor C_r is discharged by the output inductor current i_{Lo2} and the voltage across C_r decreases from the maximum value to minimum value. Then, the rippled voltage Δv_{cr} is given by

$$\Delta v_{cr} = \frac{i_{Lo2}(1-D)T_s}{4C_r} \tag{22}$$

As indicated in (21) and (22), the resonant capacitor should be large enough to reduce voltage overshoots across the rectifiers, and the resonant capacitor is defined as

$$C_r \geq \frac{i_{Lo2}(1-D)T_s}{4(V_{rec,\max} - n_2 V_{in})} \tag{23}$$

where $V_{rec,max}$ is the maximum value of voltage stresses across the bridge rectifiers.

Another consideration is that the voltage across C_r should not be discharged to zero within the desired operation range. Then, the following equation can be derived based on (22)

$$C_r \geq \frac{i_{Lo2}(1-D)T_s}{4(n_2 V_{in} - V_{o2})} \tag{24}$$

Then, (23) and (24) can be integrated as following

$$C_r \geq \max\left[\frac{i_{Lo2}(1-D)T_s}{4(V_{rec,\max} - n_2 V_{in})}, \frac{i_{Lo2}(1-D)T_s}{4(n_2 V_{in} - V_{o2})}\right] \tag{25}$$

It should be noted that the resonant capacitor C_{r1} could be relatively small comparing with C_r because there is no corresponding freewheeling interval in FB1 circuit operation.

3.4 Reduced output filter requirement

Fig. 7(a) shows the rectified voltage and output inductor current waveform of the conventional PSFB converter. The peak current ripple of output inductor can be expressed as

$$\Delta i_{1pk}(M) = \frac{k_2 V_{in} T_s}{4L_{o2}} M(1-M) \tag{26}$$

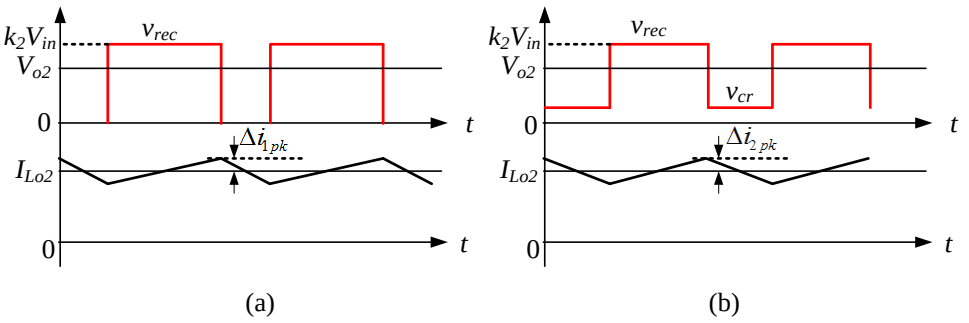

Figure 7. The rectified voltage and output inductor waveform. (a) Conventional PSFB converter. (b) The FB2 circuit.

Fig. 7(b) shows the rectified voltage and output inductor current waveform of the FB2 circuit. The peak current ripple of output inductor can be expressed as

$$\Delta i_{2pk}(M) = \frac{k_2 V_{in} T_s}{4L_{o2}} \frac{(1-M)(2M-1)}{M} \tag{27}$$

The current ripple ratio (CRR) of the FB2 circuit to the traditional PSFB converter with the same output inductance is obtained by solving (26) and (27)

$$CRR = \frac{\Delta i_{2pk}(M)}{\Delta i_{1pk}(M)} = \frac{2M-1}{M^2} \tag{28}$$

Fig. 8 shows the normalized output inductor current ripple and the current ripple ratio CRR as a function of the DC gain M. It can be seen from Fig. 9 that the output inductor current ripple in the FB2 circuit can be reduced within a wide range of DC voltage gain compared to the conventional PSFB converter. It means that the inductance in the FB2 circuit can be reduced compared to the conventional PSFB converter under the same current ripple condition.

Fig. 9 shows the key waveforms of the FB1 circuit. As shown in Fig. 10, The peak output inductor current ripple can be expressed as

$$\Delta i_{pk,Lo1} = \frac{(V_{o1} - v_{cr1})(t_{d,lagging} + t_{d,loss})}{2L_{o1}} \tag{29}$$

where $t_{d,loss}$ is the duty cycle loss of the FB1 circuit, and $t_{d,loss}$ is given by

$$t_{d,loss} = \frac{L_{lk1}(k_1 i_L - I_{Lm1})}{V_{in}} \tag{30}$$

where i_L is the load current of the proposed converter. As indicated in (18), (29) and (30), the time intervals $t_{d.lagging}$ and $t_{d,loss}$ are small enough so that the output inductor current ripple is very small. This means that the inductance L_{o1} can be designed to be very small at the given output inductor current ripple condition, allowing compact output inductor size.

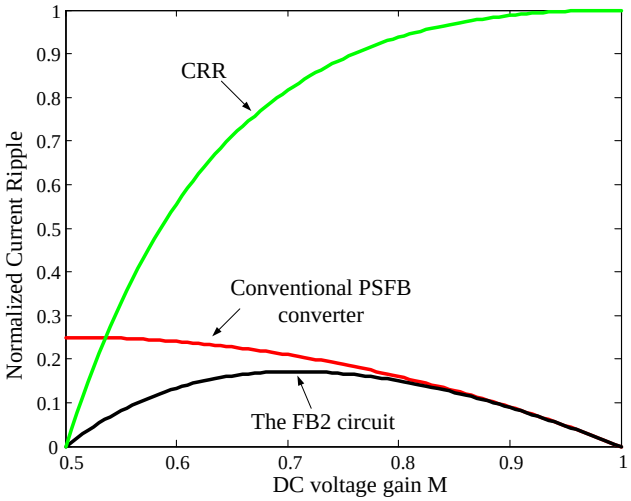

Figure 8. Normalized output inductor current ripple and the output current ripple ratio CRR versus DC voltage gain M.

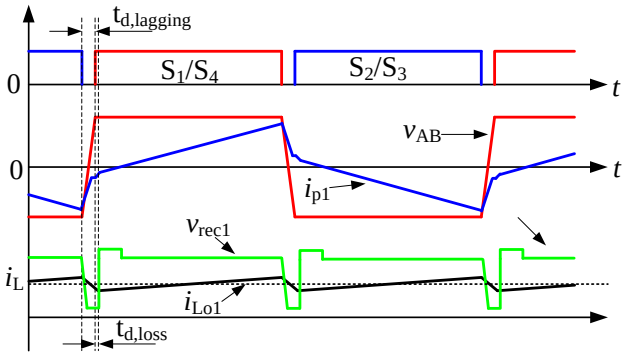

Figure 9. Key waveforms of the FB1 circuit

4 Experiment results and discussions

A 1-kW hardware prototype of the proposed converter has been designed, made and tested to verify the circuit operation principles. The prototype converter has the following specifications: input voltage V_{in} = 90-110V; output voltage V_o =500-700V; switching frequency f_s = 100kHz. The circuit parameters are illustrated in Table II. Fig. 10 shows the schematic diagram of experimental circuit. In this scheme, the FB1 circuit can also be regulated by phase-shift control so that the output voltage can be brought lower than the normal minimum voltage for which the converter is designed, and therefore the device current during start-up and overload conditions can be effectively limited by this arrangement. As shown in Fig. 10, the control circuits of the proposed converter are based on the conventional phase-shift control IC UC3895. The two UC3895s are synchronous with each other, and a simple logic gate array (LGA) is employed to cope with the two random situations, which are analyzed in [34]. The control voltage v_c in Fig. 10 is based on the error between the actual and desired output voltage, and is designed to vary from 5V to 10V under normal operating conditions. Hence, UC3895-1 operates with full pulse-width and the pulse-width of the FB2 circuit is adjusted to control the output voltage. Under start-up and overload conditions, the control voltage falls below 5V, hence the pulse-width of the FB1 circuit is controlled now, and the FB2 circuit operates with zero pulse-width. Therefore, the device currents can be limited under start-up and overload conditions by this arrangement. A photograph of the experimental prototype is shown in Fig. 11.

Fig. 12 shows the key waveforms of the FB2 circuits for three different modes. It can be confirmed from this figure that the primary circulating current has been significantly reduced in all operation modes. Meanwhile, there is no voltage spikes across the secondary-side diodes of the FB2 circuit. Fig. 13 shows the key waveforms of the FB1 circuit at V_o =600V and P_o = 1000W. It can be confirmed from the measured waveforms that the there is also no voltage spikes across the secondary rectifiers of the FB1 circuit. In consequence, diodes with lower breakdown voltage rate, better reverse recovery characteristic and lower forward voltage drop can be used, and this can reduce conduction loss and reverse recovery loss of the secondary rectifier. Hence, the proposed converter would be useful for high output voltage and high power applications.

Figs. 14 and 15 show the switching waveforms of S_1 and S_3 with the same output voltage (600V) for different load conditions. It can be clearly demonstrated that ZVS of the lagging leg switches in the proposed converter can be actually realized for all power range. Fig. 16 shows the loss evaluation for several main parts of the proposed converter with the same output voltage for different output power according to the parameters in Table II. As shown in Fig. 16, the conduction losses of power devices and the copper losses of transformers dominate the main parts of the power loss breakdown, and therefore the effect of utilizing the soft-switching technologies is confirmed herein. The measured efficiency with different loads and different output voltages is given in Fig. 17. It can be seen that, high efficiency over wide load range is achieved and the peak efficiency achieves 95.5% under 1-kW

output power and 700-V output voltage conditions. The conduction losses of the active switches and output diodes are reduced with lower current stresses leading to better efficiency with a higher output voltage.

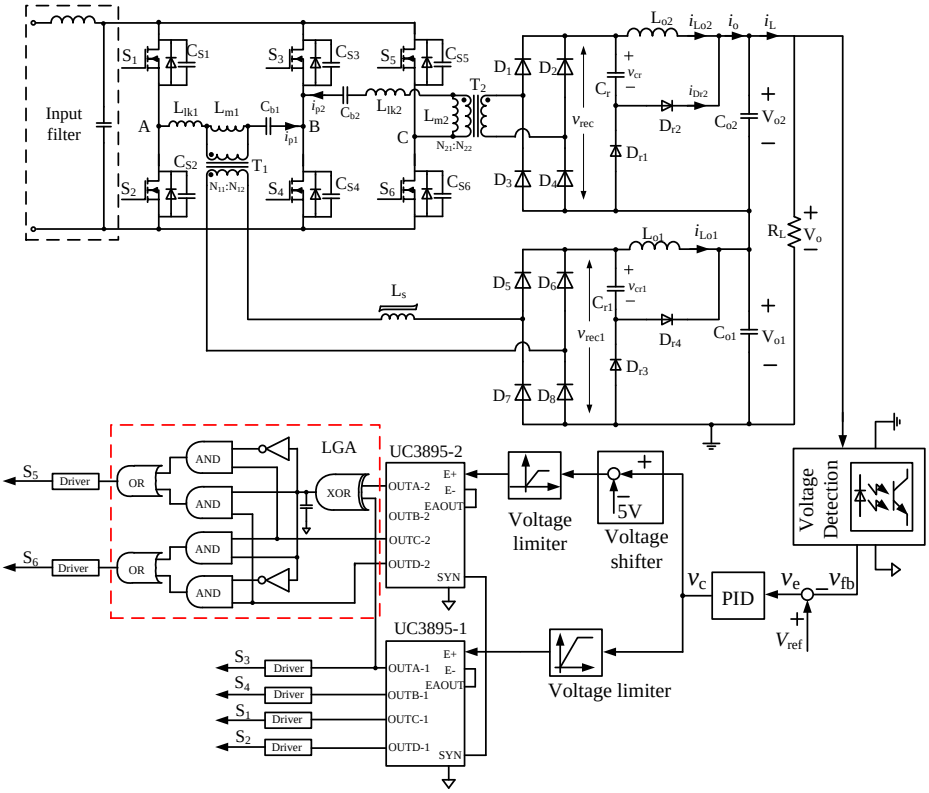

Figure 10. Schematic diagram of the laboratory prototype

Table 2. Circuit Parameters

Components	Parameters
Transformer T_1	Ferroxcube E42/21/15-3C95 ferrite core; Primary turns N_{11}=14, Secondary turns N_{12}=49; Magnetizing inductance L_{m1}=40uH; Leakage Inductance L_{lk1}=2.5uH
DC Blocking Capacitor C_{b1}&C_{b2}	15uF, 250V high-frequency film capacitor
Output Inductance L_{o1}	Arnold MS-092060-2 Sendust core turns N=41, L_{o1}=85uH
Transformer TR2	Ferroxcube E42/21/15-3C95 ferrite core; Primary turns N_{21}=14; Secondary turns N_{22}=80; Magnetizing inductance L_{m1}=1mH; Leakage Inductance L_{lk1}=6.4uH
satuable Inductance L_s	Ferroxcube TN9/6/3-3R1 ferrite core turns N=7
Output Inductance L_{o2}	Arnold MS-130060-2 Sendust core turns N=79, L_{o1}=382uH
Output Capacitor C_{o1}&C_{o2}	4.7uF, 630V high-frequency film capacitor
Primary Switches S_1-S_6	International Rectifier IRFP90N20D, 200V, 94A. $R_{ds,on}$=0.023Ω
Output Diodes D_1-D_8	Infineon SiC Schottky diode IDW30G65C5 650V, 30A
Diodes D_{r1}-D_{r4}	Fairchild ultrafast diode MUR1560 600V, 15A
Resonant capacitor C_r&C_{r1}	33nF, 1200V high-frequency film capacitor

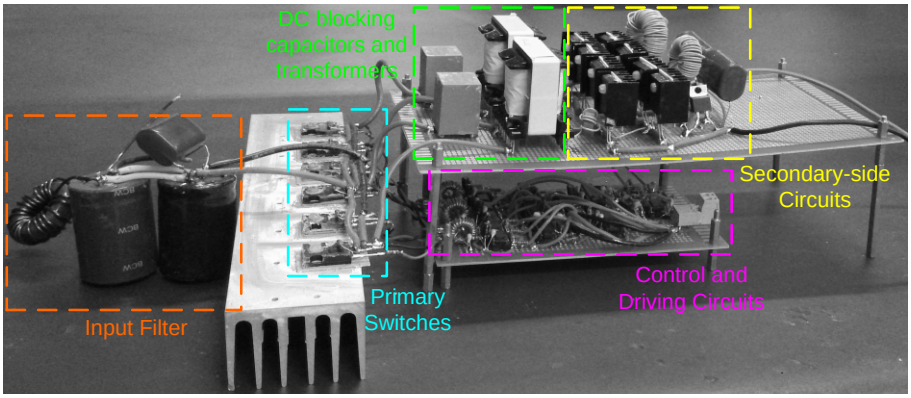

Figure 11. Experimental prototype

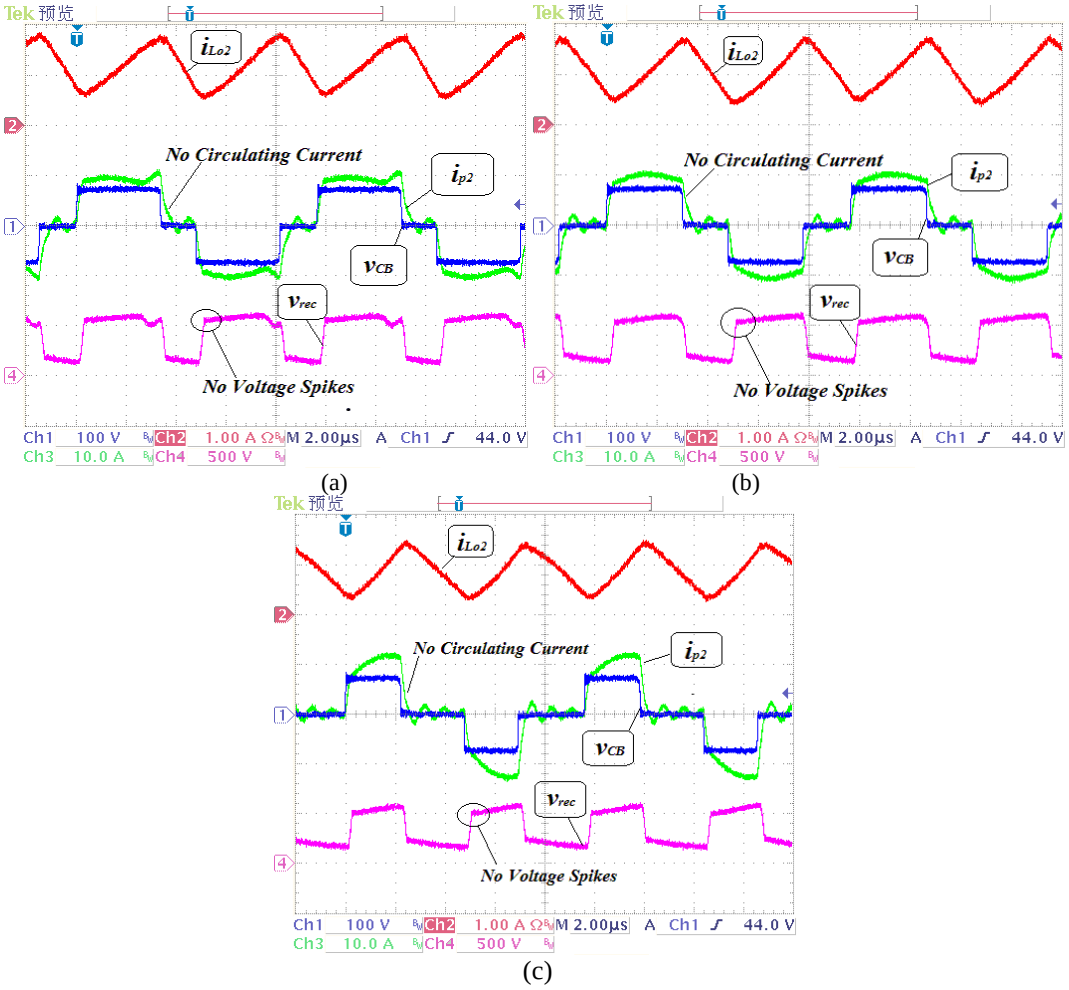

Figure 12. Key waveforms of the FB2 circuits for three different modes: (a) Mode 1 at D = 0.75, (b) Mode 2 at D=0.67, (c) Mode 3 at D=0.46.

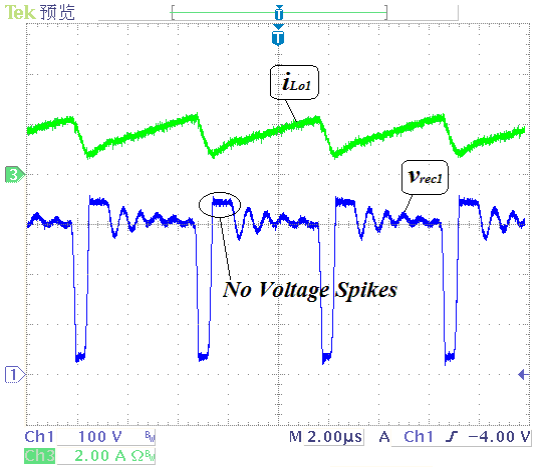

Figure 13. Key waveforms of the FB1 circuit at Vo=600V and Po=1000W.

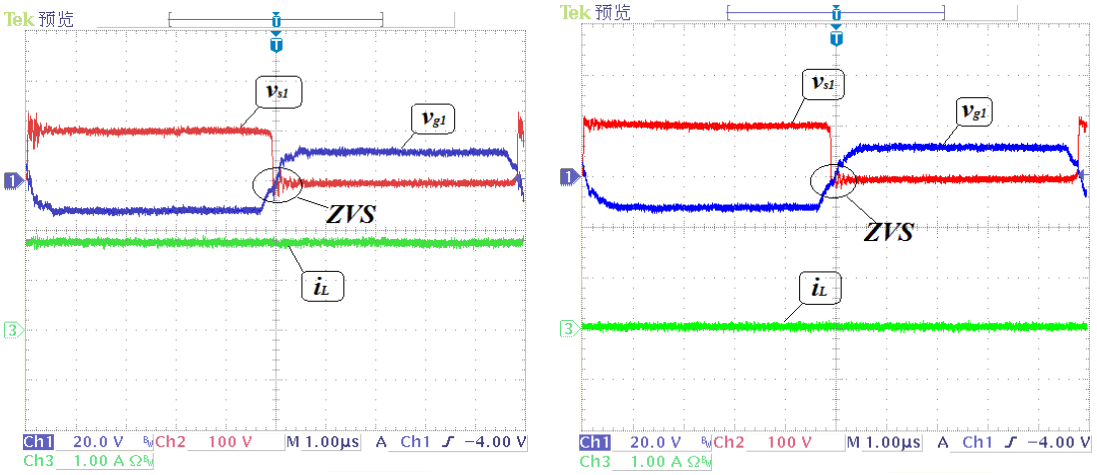

Figure 14. Measured switching waveforms of S1 with different load conditions: (a) Po=1000W, (b) Po=20W.

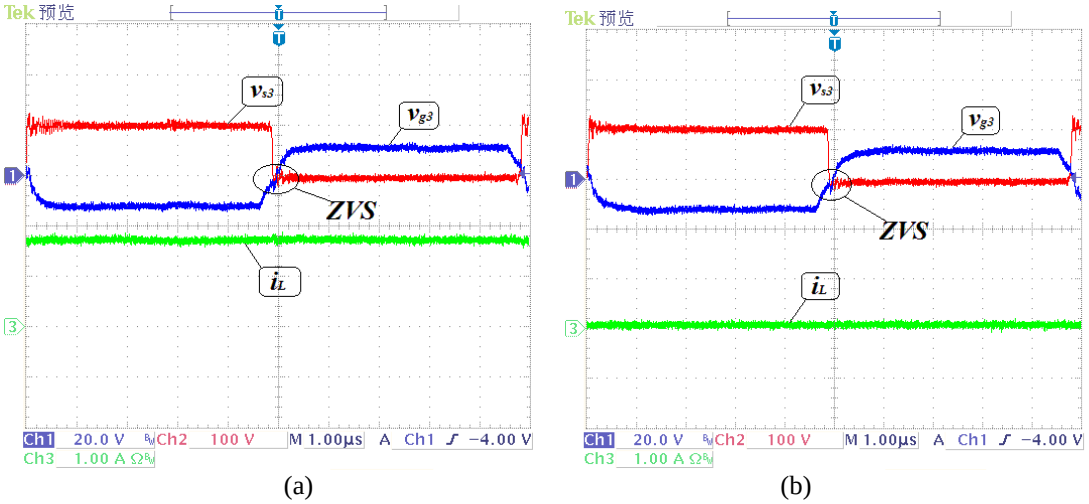

Figure 15. Measured switching waveforms of S3 with different load conditions: (a) Po=1000W, (b) Po=20W.

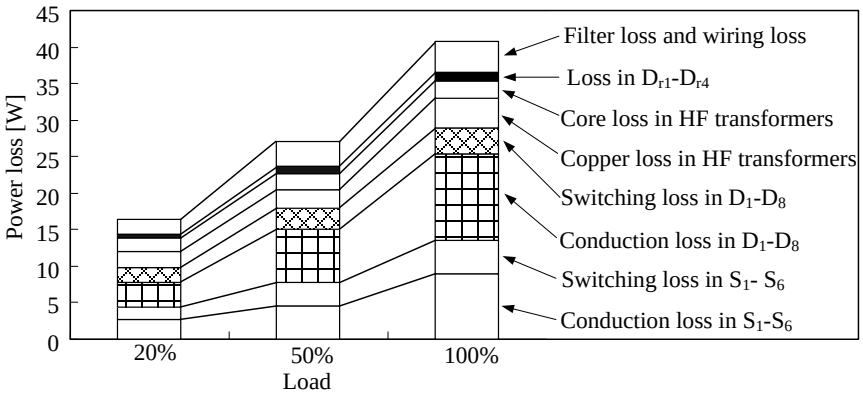

Figure 16. Loss evaluation for different load conditions with Vo = 600-V.

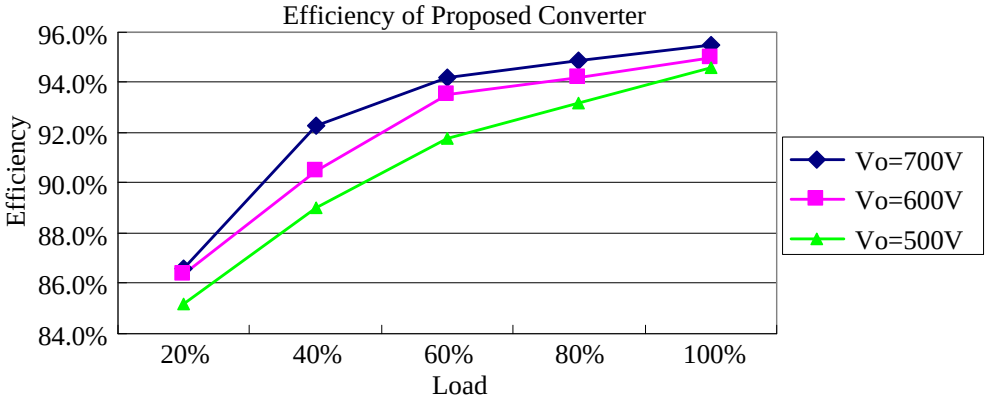

Figure 17. Experimental results of efficiency at different loads and different output voltage.

4 Conclusion

This paper presents a novel dual full-bridge converter with shared lagging leg and dual outputs in series. ZVS of the lagging leg switches in the proposed converter is realized for all power range by using the magnetizing current of transformer. The secondary-side resonant circuit can effectively reset the primary-side circulating current, as well as clamp secondary rectifier voltage. The voltage stresses across the output terminal power devices are greatly reduced because of the dual outputs in series configuration. In consequence, rectifiers with lower breakdown voltage rate, better reverse recovery characteristic and lower forward voltage drop can be used, and this can reduce conduction loss and reverse recovery loss of the secondary rectifier. Hence, there is great potential for this converter to be used for high voltage and high power applications. Experimental results obtained from a laboratory-made prototype have been presented to demonstrate the performance of this converter.

Acknowledgements

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