# Control Strategy And Experimental Research of 10kV Power Quality Disturbance Integrated Device

Haifeng Huang<sup>1, a</sup>, Wei Fu<sup>1, b</sup> and Xiaofei Chen<sup>2, c</sup>

<sup>1</sup>State grid Hubei energy service Co., Ltd., Wuhan,430077, China.

<sup>2</sup> Nari(Wuhan) electrical equipment &engineering efficiency evaluation center, Wuhan 430074, China.

<sup>a</sup>181259409@gg.com, <sup>b</sup>283727819@gg.com, <sup>c</sup>924097382@gg.com

**Keywords:** Power Quality, disturbance, harmonic, three-phase unbalance, integrated device.

**Abstract.** A power quality disturbance integrated device is proposed which can simulate the voltage and current disturbance of the power system, the output of the device include voltage sag, voltage fluctuation and flicker, voltage harmonic, current harmonic, three-phase voltage and current unbalance and so on. The output of the device has good waveform, large power and high voltage level. The device adopts the multi-winding transformer +Voltage Source PWM Rectifier + cascade multilevel inverter structure. The control strategy of the PWM Rectifier is dual-loop control, with good input current waveform and stable dc voltage. Based on carrier phase shift cascade multi-level inverter, the control strategy of the inverter is voltage feed-forward with repetitive learning, and the high accuracy output is achieved with the high precision output waveform. A simulation model based on PSCAD / EMTDC software platform is developed and the 1.5MVA / 10kV Power quality disturbance integrated device is developed. Simulation and experimental results verify the correctness of the main circuit topology and control strategy.

#### 1. Introduction

With the rapid development of power electronic devices and related control technologies, a large number of power electronic device is applied to the power system, power quality problems resulting growing[1,2,3]. With the outstanding of power quality problems and the development of power quality control equipment, the traditional means of testing electrical equipment encountered challenges. so, there is an urgent need for a power quality disturbance generator which can test the electrical equipment for power quality problems tolerance.

In[4]it is proposed a multi-target voltage disturbance generator, with a voltage disturbance generation function, the fundamental and harmonic generation module separately controlled; Literature[5] proposed a cascade type disturbance current generating device, which can generate variety kinds of current waveforms, the device uses a three-phase full-bridge rectifier, inverter side in series in the form of H-bridge power unit; Literature [6] proposed a power quality signal generating device based on dual PWM inverter and voltage hysteresis control, and the main function is voltage disturbances. On the basis of previous research, this article proposed a 10kV power quality disturbance integrated device with the structure of multi-winding transformer +Voltage Source PWM Rectifier + cascade multilevel inverter, the device can simulate a variety of power quality disturbance waveform output which include voltage disturbance and current disturbance ,by switching mode of the device.

The basic module of the main circuit is single-phase back to back H-bridge structure, each phase of 14 units cascade, cascade multilevel structure is used in inverter side which can improve the output voltage level. After adopting this structure, the device equivalent switching frequency can theoretically improve to 2N times of IGBT switching frequency[6,7,8] (N -each phase cascade unit number), the quality of output waveform can be Improved. Multi-winding transformer used in rectifier side, which can effectively prevent the mutual coupling on the magnetic circuit of PWM rectifier. PWM rectifier transformer adopt pair of parallel connection mode, then through the

transformer winding access to system, the control strategy using triangular carrier phase shifting control, to ensure that the injection system switch ripple is greatly reduced, the current draw from the system as a sine wave.

## 2. Main Circuit Topology

The main topology of the 10kV power quality disturbance integrated device is shown in figure 1, It consists of three phase power system, multi-winding rectifier transformer, back-to-back power unit, connect reactor, filter, etc. The secondary side of the Multi-winding rectifier transformer connected to the AC side of each rectify unit, reducing the rectifier input AC voltage level . Voltage source PWM rectifier(VSR) not only provide stable DC bus voltage to the inverter unit, but also make the rectifier be run in the condition of unity-power factor. Since the PWM rectifier can achieve the four-quadrant operation, the active power of the inverter can be feedback into the power networks, or provide active power to the load by the inverter, and the control strategy through the DC bus voltage control to achieve energy feedback and provide. Under the mode of voltage disturbance, by controlling the inverter output voltage, output voltage disturbance waveform; in the current mode, one end of the tested equipment connect to the output end of the device, another end of the tested equipment connect to the 10 kV system, by controlling the inverter output voltage, output current disturbance waveform.

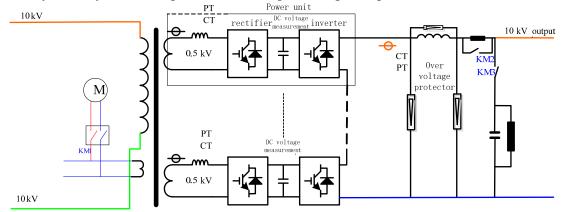


Fig. 1 Main topology of the power quality disturbance integrated device

## 2.1 Equivalent model of the voltage disturbance mode.

Under the mode of voltage disturbance, the tested equipment connect to the output end of the device through the RLC filter. By adjusting the output voltage of the device, the voltage of the tested equipment can be changed. The equivalent model of the voltage disturbance mode is shown in figure 2:

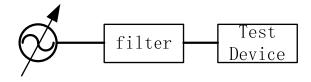


Fig.2 Equivalent model in voltage mode

If only considering the fundamental and harmonic under 50 times, and the filter circuit can effectively filter out switch ripple, the device output voltage  $u_o$  is:

$$u_o = Nu_{dc} \sum_{k=1}^{50} m_k \sin(k\omega_s t + \varphi_k)$$
 (1)

Where, N is cascade unit number;  $u_{dc}$  is the DC voltage of Back-to-back power unit; k is harmonic number;  $m_k$  is modulation ratio of kth harmonic (k is a integer);  $\varphi_k$  is initial phase of kth harmonic (k is a integer).

#### 2.2 Equivalent model of the current disturbance mode.

From voltage mode analysis, the disturbance device can be equivalent to a controllable voltage source, in current source mode, the tested equipment connect between the 10kV network and the controllable voltage source, by controlling the inverter output voltage, so as to control the current of the tested equipment. The equivalent model of the current disturbance mode is shown in figure 3:

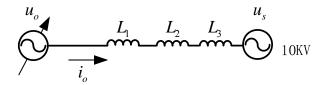


Fig.3 Equivalent model in current mode

Where,  $L_1$  is filter reactance,  $L_2$  is the reactance of output transformer,,  $L_3$  is the reactance of the tested equipment,  $u_o$  is output voltage of the disturbance device,  $u_s$  is the network voltage,  $i_o$  is the output current, then:

$$i_o = \frac{u_o - u_s}{(L_3 + L_2 + L_1)j\omega}$$
 (2)

 $u_s$  is a constant value,  $u_o$  is a variable, by changing  $u_o$  that is realized with the adjustment of the current, so as to realize the current mode.

### 3. Control Strategy of The Device

The control objective of the rectifier part of the power quality disturbance device is to stabilize the DC voltage of the inverter bridge, at the same time, the rectifier bridge works in the unit power factor; the control objective of the inverter is to output various power quality disturbances, including voltage harmonics, voltage sag, voltage fluctuation and flicker, current harmonics, etc. The various kinds of disturbance signals generated by the chip as the instruction signal, PWM modulation of the inverter is obtained by proper control of the voltage, After comparing the fixed frequency triangular carrier with the modulation wave, the gate trigger signal to control the IGBT turn-on and turn-off is obtained. control of the IGBT is controlled by the gate electrode and the gate electrode, then by controlling the output of the inverter, the device output the target disturbance waveform. As shown in Figure 4, is the main circuit of the back-to-back power unit. The power unit consists of PWM rectifier bridge and PWM inverter bridge, where L is input side filter reactance;  $C_1 \times C_2$  is the DC storage capacitor, by parallel connection to increase the capacity of the capacitor; R is equalizing resistance, It can provide the release channel for the energy;  $u_{ac}$  is DC-side voltage;  $u_i$  is input voltage of the rectifier bridge;  $u_o$  is output voltage of the inverter bridge;  $u_o$  is output voltage of the inverter bridge.

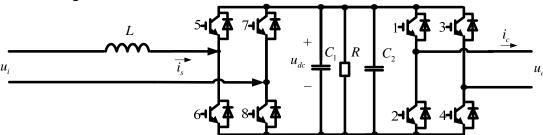


Fig. 4 Main circuit of back-to-back power unit

#### 3.1 Control strategy of rectifier bridge

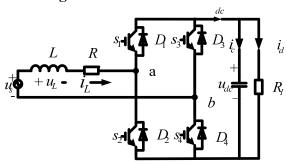


Fig.5 Equivalent circuit diagram of the back-to-back power unit

Figure 5 is a back-to-back power unit rectifier equivalent circuit diagram, the control objective of the rectifier bridge is to stabilize the DC side voltage of the PWM rectifier in the setting value, and enable the PWM rectifier to run in the condition of unity-power factor. The control strategy is composed of two loops which is a outer voltage loop and inner current loop, the outer voltage loop is rectifier DC voltage control loop, the inner current loop is rectifier AC current control loop[5], the control block diagram is shown in Figure 6,the control principle is as follows: neglect of harmonic interference, In practice,  $u_{dc}$  contains DC component and pulsating AC component, The AC component is small and not easy to control, So the control of the  $u_{dc}$  is usually transformed into the control of the DC component  $\overline{u}_{dc}$ . The implementation method is using sliding window to get the average value of the DC voltage in a period,  $\overline{u}_{dc}$  compared with DC voltage reference value, the D-value regulated by PI regulator, the output of the PI regulator is a DC signal, and the phase of the sinusoidal signal is obtained by the phase locked loop. Multiply this DC signal with the which has the same phase with the grid voltage, and this sine signal is obtained by phase-locked loop, then got the reference current of the rectifier  $i_{ref}$ ,  $i_{ref}$  compared with the AC side inductor current  $i_L$ , by the PI regulator, then obtain the modulating signal  $u_{m1}$ , ensure the input voltage can be tracked with zero steady-state error by the inductor current. In order to make dc voltage control effect is more stable, still need to add voltage feed forward control, Multiply  $u_s$  with scaling factor  $k_z$ , then got the modulated signal  $u_s k_z$  (  $k_z$  is grid-connected parameter of PWM rectifier), adding  $u_{m1}$  and  $u_s k_z$ together, then the PWM modulated wave signal can be obtained. The device adopts the technology of single pole frequency doubled sinusoidal pulse width modulation (SPWM), that is, the IGBT of the different bridge arm uses the opposite phase modulation wave, compared with the same triangular carrier, then got the IGBT drive signal, make the rectifier output target voltage[6].

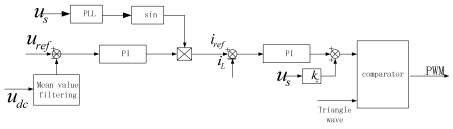


Fig. 6 Double loop control block diagram of the rectifier

Considering the inner current loop sample delay, small inertia characteristics of PWM control, and the grid voltage disturbance, the current inner loop structure is shown in Figure 6[7]:  $T_c$  is the current sampling period of the inner current loop(also the PWM switching cycle).

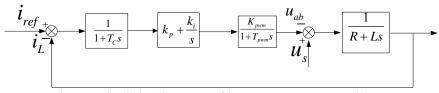


Fig. 7 Principle diagram of inner current control loop

Voltage source PWM rectifier can be equivalent to the amplification of pure hysteresis,  $K_{pwm}$  is the gain,  $T_{pwm}$  is the lag time of PWM modulation, take the value of  $0.5\,T_c$ , in consideration of the current inner loop need a quickly current following performance, the typical I model is used to design the controller parameters[8], as is shown in Figure 6, make the zeros of the PI controller cancel the poles of the current control transfer function, that is  $\tau_i = \frac{k_p}{k_i} = \frac{L}{R}$ . After correction, the current inner loop

transfer function is

$$G_{oi}(s) = \frac{k_p k_{pwm}}{Ls(1.5T_c s + 1)}$$
(3)

The parameter tuning is performed based on typical I model[9], when the system damping  $\xi$ =0.707,then:

$$\frac{1.5T_c k_p k_{pwm}}{R\tau_i} = \frac{1}{2} \tag{4}$$

$$k_p = \frac{R\tau_i}{3T_c k_{pwm}}, k_i = \frac{R}{3T_c k_{pwm}} \tag{5}$$

The current inner loop PI control parameters can be obtained by the above formula and related rectifier parameters., and the voltage outer loop can be designed with similar method.

## 3.2 Control strategy of inverter bridge

The main function of PWM inverter bridge is to generate a given voltage or current instruction signal, and achieve the output of the disturbance device. Cascaded carrier phase shifted unipolar frequency doubled sinusoidal pulse width modulation (CPS-SPWM) be used in inverter side, cascade of 14 units per phase, each inverter unit uses the same modulated wave signal- $u_s(\omega_s t)$ ,  $\omega_s$  is angular frequency of modulated wave signal,  $k_c\omega_s$  is the carrier frequency of the inverter unit, the carrier frequency of each unit is the same, but the inverter unit carrier phase offset, Followed by the phase difference of the 1/14carrier cycle, so the phase angle of the L inverter(L is the serial number) is  $\varphi_L = \varphi_C + 2\pi L/14$ , the output waveform of the cascaded inverter is the Superposition output waveform of the inverter unit[10,11,12,13]. Total output voltage of the inverter is multi level stepped wave, can significantly reduce the output voltage change rate stress and output voltage and current harmonic content[10,14,15]. According to the functional classification of the device, control strategy of the inverter is divided into voltage mode control strategy and current mode control strategy.

## (1) Voltage mode control strategy

Voltage mode control strategy for PWM inverter bridge is shown in Figure 8. Compare instruction voltage  $u_c^*$  with output voltage  $u_c$ , use repetitive learning controller to the deviation quantity, then obtain the modulated wave  $V_m$ , after a CPS-SPWM modulation, the target voltage  $u_c$  can be output through the cascade structure and the filter circuit. Repetitive learning control can effectively eliminate the periodic error caused by periodic disturbance, so as to improve the output tracking effect[10,14,15].

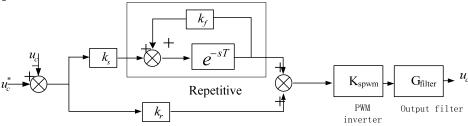


Fig 8 Control principle of PWM inverter bridge in voltage mode

## (2) Current mode control strategy

Current mode control strategy for PWM inverter bridge is shown in Figure 9. The target output of the current mode control is the current, but in the higher harmonics, the current will produce a large voltage drop on the connecting reactor, So as to affect the actual output, therefore need to add the appropriate amount of compensation; in addition, the current mode is added to the function of continuous power factor. Control principle is as follows: the device synthesized instruction current  $i_c^*$  according to the required disturbance, at the same time, according to the target power factor can be active and reactive power commands  $P_{ref}$  and  $Q_{ref}$ , compared with actual output active power and reactive power respectively, after PI regulation, then the dq inverse transform, get the current signal  $i_f$ , the sum of  $i_c^*$  and  $i_f$  is compared with the output current  $i_c$ , use repetitive learning controller to the deviation quantity, then obtain the modulated wave  $V_{m2}$ ; at the same time, the compensation  $V_{m3}$  can be obtained by multiplying  $i_c^*$  with connection impedance. The feed forward control can be added, and the feed forward quantity  $V_{m4}$  contains two parts, which is in phase with the input voltage  $(k_{p5}u_s)$  and ahead of the input voltage of 90  $^{\circ}(k_{p6}u_{s\perp})$ ; add  $V_{m2}$  and  $V_{m3}$  are  $V_{m4}$  together, can get the final modulation signal  $V_{m1}$ , after a CPS-SPWM modulation, the target current  $i_c$  can be output.

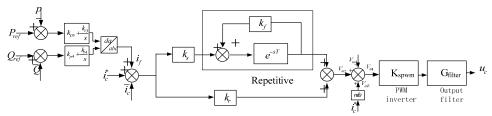


Fig 9 Control principle of PWM inverter bridge in current mode

#### 4. Simulation Analysis Based on PSCAD

In order to verify the feasibility of the design and control strategy of the main circuit parameters of the device, build a simulation model in PSCAD, cascade of nine units per phase. The system includes power supply, back-to-back power unit, filter, control module etc.. The simulation parameters are as follows: the unit DC voltage setting value is 800V, the rectifier side input voltage is 450V, switching frequency is 6000Hz, DC side capacitor is 4200  $\mu$  F, output filter reactance is 0.8mh, output filter capacitor is 1  $\mu$  F. The simulation waveforms are shown below:

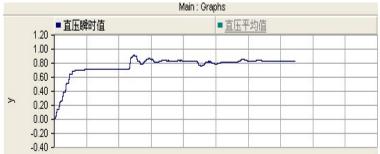


Fig. 10 Simulation waveforms of the Dc voltage of PWM rectifier

Set the fundamental output 5kV to stack the 15th harmonic 0.8kV, waveform is shown in Figure 11:

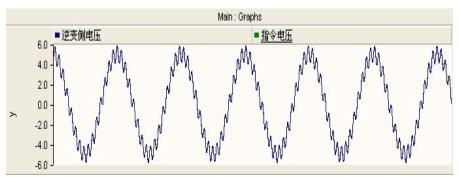


Fig.11 Waveform of fundamental wave 5kV with the 15 harmonic 0.8 kV

The simulation waveforms show that the control method can Control method can accurately track the setting waveforms, and can be used to guide the hardware design.

# 5. Experimental Research

On the basis of theory and simulation, the device is developed, as shown in Figure 12.



Fig.12 Physical map of the device

Voltage disturbance and current disturbance experiments have been done on the device, PS-8 power quality tester and fuluk1750 power quality analyzer are used to measure and record. The experimental waveforms are shown in the following figs:



Fig.13 Waveform and frequency spectrum of fundamental 8kV + 7th harmonic 2 kV + 23th harmonic 2 kV

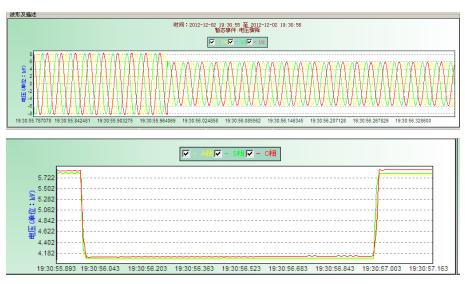


Fig.14 Three-phase voltage output waveform of Sag depth 30% Sag time 1s

The experimental waveforms of the voltage mode are shown in Figure 13 and 14, when the tested device is pure resistive load, can be seen from the figures that when the reference output waveform is fundamental 8kV + 7th harmonic 2 kV+23th harmonic 2 kV, the output can track the input; when the reference output waveform is voltage sag(sag depth 30%,sag time 1s), the device can accurately output the voltage sag, and the sag depth and sag time are close to the setting value, the experimental results indicate that this equipment can be used to determine the sensitivity of electrical equipment to voltage sag.

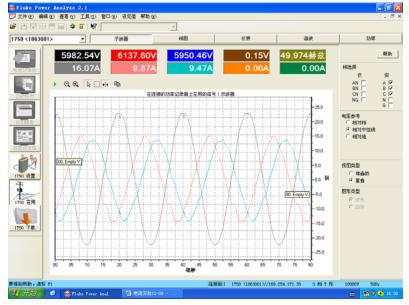


Fig.15 Waveform of Three phase current unbalance degree 50%

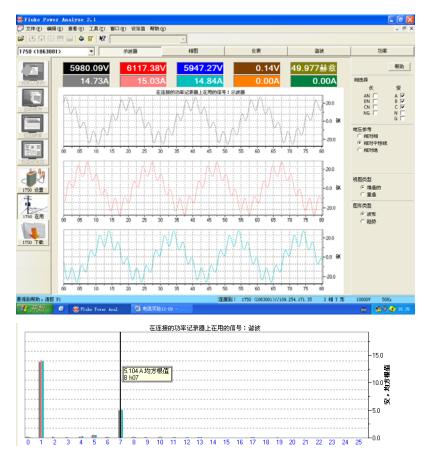


Fig.16 Waveform and frequency spectrum of fundamental wave 15 A +7th harmonic 5A

The experimental waveforms of the current mode are shown in Figure 15 and 16, the tested device is a three-phase transformer. Figure 15 shows the waveform of the three-phase current unbalance (30%); Figure 16 shows the waveform and frequency spectrum of fundamental wave 15 A +7th harmonic 5A.

The experimental results show that the control strategy and circuit design are correct and effective, the device is capable of accurately outputting the required voltage and current disturbance waveforms, can accurately simulate the power system's various power quality problems.

## 6. Summary

On the basis of theoretical and simulation analysis, this paper studies the 10kV power quality disturbance integrated device, the experimental apparatus was developed, the voltage and current double loop control for the rectifier can accurately stable DC voltage at the reference value, the rectifier AC side current waveform is good, and running on the condition of the unit power factor; the control strategy based on the output feedback, the reference waveform forward and the repetitive learning control is used in the inverter side, can accurately track the reference waveform, the inverter side of the carrier phase cascade multilevel to further improve the accuracy of the output waveform. Through the acquisition of experimental waveforms, the feasibility of main circuit structure and control strategy of power quality disturbance integrated device is further verified.

#### References

- [1]. Jos Arrillaga. Power System Harmonics [M].
- [2]. Dong-Jun Won, Seon-Ju Ahn, II-Yop Chung, et al. A new definition of voltage sag duration considering the voltage tolerance curve [J]. IEEE Bologna PowerTech Conference, 2003: 23-26.

- [3]. Kjolle, G.H., Seljeseth, H., Heggset, J., et al. Quality of supply management by means of interruption statistics and voltage quality measurements[J]. European Transactions on Electrical Power, 2003, 13(6):373-379.
- [4]. CAO Song-wei, YIN Zhong-dong. Study of Multi Objectives Voltage Disturbance Generator Based on Carrier Phase Shift[J]. Power Electronics, 2012,47(7):92-95.
- [5]. ZHAO Xiaoying, ZHAO Ruibin, ZHANG Yibo. Design of Cascaded Current Disturbance Generator[J]. Electronics & Packaging, 2013,13(1):30-33,37.
- [6]. Liu Qiao, Yin Zhongdong, Hong Qiu, et al. Series-connected hybrid cascaded H-bridge voltage disturbance generator[C]. 2009 International Conference on Energy and Environment Technology, Guilin, China, 2009.
- [7]. Chung Y H, Kwon G H, Park T B. Voltage sag and swell generator with thyristor controlled[C]. International Conference on Power System Technology, Kunming, China, 2002.
- [8]. Lee Y H, Park H Y, Nho E C, et al. Improved voltage disturbance generator for the performance test of the custom power devices[C]. International Conference on Electrical Machine and Systems, Seoul, Korea, 2007.
- [9]. ZHAO Jian-feng, WANG Xun, PAN Shi-feng. Dual PWM Converter and Voltage Hysteresis Control Based Power Quality Signal Generator[J]. Power System Technology, 2005,29(4):40-44.
- [10]. Girgis A A, Makrarn E B, Baldwin T L. Computer-based harmonic generator facilities to study harmonic related problems[J]. IEEE Trans on Power Systems, 1989, 4(3): 1252-1257.
- [11]. ZHAO Bo, GUO Jian-bo, ZHOU Fei et al. Design of A Novel Multi-Functional 10kV Voltage Disturbance Generator[J]. Power System Technology, 2010, 34 (8): 75-80.
- [12]. Jewell W. Power quality laboratory testing[C]. IEEE Power Engineering Review, Kansas, USA, 2002.
- [13]. Pekik Argo Dahono , Yogi Rizkian Bahar , Yukihiko Sato , et al. Damping of transient oscillations on the output LC filter of PWM Inverters by using a Virtual Resistor[C]//2001 4th IEEE International Conference on Power Electronics Drive Systems, 2001: 403-407.
- [14]. Nho E C, Kim L D, Park S D, et al. Reduced voltage drop characteristics of the series transformer in a voltage disturbance generator[C]. The 7th International Conference on Power Electronics, Daegu, Korea, 2007.
- [15]. ZHOU Fei,QIAO Guang-yao,ZHAO Rui-bin, et al. Control Strategy Study of Current Disturbing Device[J]. Power Electronics, 2010,44(8):29-31.