Design of high-accuracy decimal frequency divider with Verilog-HDL

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Abstract. This paper presents a more complex algorithm with Verilog-HDL, which based on the dual-modulus preseted decimal frequency divider. This algorithm can not only increase the accuracy of decimal frequency divider. , but also can be used to divide a clock. Simulations are conducted to analyze the characteristics of the decimal frequency divider and DDS divider. The results shows that the divider can satisfy the requirements of design.

I. INTRODUTION

In the 21st century the development of digital integrated circuits become more and more important in the design field of IC. Compared with the analog circuits, digital circuits show great advantages in power consumption. And algorithm of digital circuits is easy to implement. Therefore, the study of digital circuits becomes very significant [1].

As we all know, the digital systems can work normally according to a beat. The beat is the signal of clock which is generated by a clock circuit. The clock circuit is composed of crystal oscillator. The crystal oscillator can provide a stable clock. However, this clock is always different from the required clock which is based on the frequency of input clock. It's necessary to design a frequency divider to divide the input clock into different frequencies and assign the divided clock to the other modules. To sum up, the design of the frequency synthesizer becomes the most basic and most critical part of the digital IC design.

The divider is a very important basis part of the digital IC design [2-3]. And the integer frequency divider is easy to achieve. But in most instances, the frequency division ratio is not an integer number. In this case we need a fractional divider to divide the input clock.

Now the fractional divider can be implemented mainly by the following ways: 1）the Phase-locked Loop frequency synthesizer. 2）Direct Digital Synthesizer. Both frequency synthesis modes can get a precision performance. However, both frequency synthesis methods would consume a lot of circuit resources. Therefore in some circumstances, such as the circuit's resources are scarce relatively, the circuit needs a low-power clock. In such cases, the digital programming fractional divider can be used.

Because of the above idea, this paper proposes a high-precision fractional divider that based on Verilog-HDL, which can reach a reliable division results. And at the end of the paper a comparison between the fractional divider and DDS is presented.

II. THE ALGORITHM OF HIGH-ACCURACY DECIMAL FREQUENCY DIVIDER

A. Design Principles

The core idea of this design lies in the dual-modulus decimal frequency division, which means to overcount or undercount a pulse to get the decimal frequency value on average [4]. Provided that K is the decimal value of crystal frequency-output frequency ratio, K can be expressed as:

$$K = N + \frac{A}{B} \qquad (1)$$

Where N represents the integral part of K, andA/B represents the decimal part of K.A is less than B. When frequency coefficient K is a n-bits decimal number, B equals 10n. If N+1 decimal frequency is just conducted for B times and then N decimal frequency is carried out for the rest of B-A times, the output of frequency divider will not be the proper decimal frequency division on a small scale, and frequency divider will be encountered with serious phase jitter. Therefore, in order

to achieve high-accuracy decimal frequency division, an appropriate method is needed to distribute the N decimal frequency and N+1 decimal frequency better, by which the satisfactory output frequency will be obtained.

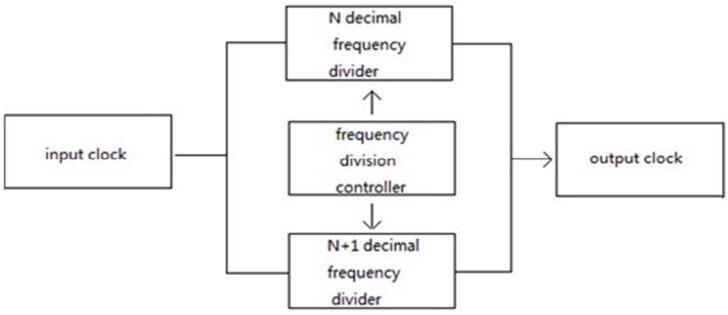

Figure 1. Schematic Diagram of High-Accuracy Decimal Frequency Divider

As is shown in Figure 1, the core of decimal frequency divider designed in this paper is the design of frequency division controller. It's main idea is that in each round, twice dual-modulus decimal frequency divisions will be made to the short-range clock and long-range clock produced. Through this the twice dual-modulus decimal frequency divisions can get a short-range clock whose cycle is shorter than the objective output clock and a long-range clock whose cycle is longer than the objective output clock respectively. The cycles of short-range clock and long-range clock gained in each round tend to be closer to the objective output clock than that are in the last round. If do this a round after a round, moreover, after enough rounds, the final errors of output clock can be controlled in a small range, so the engineering requirements can be met.

B. Parameter Algorithm

This paper conducts the design of frequency divider based on four rounds of frequency division, and as indicated in the Formula, the error of frequency μ produced in each round can be expressed as:

$$\mu = C_A E_A + C_B E_B \qquad (2)$$

Where CA is the cycle number of N frequency division in a round (it can be noted as the number of short cycle), CB is the cycle number of N+1 frequency division in a round (it can be noted as the number of long cycle); EA is the error of the frequency between the clock got by N frequency division and the output frequency, and EB is the error of the frequency between the clock got by N+1 frequency division and the output frequency.

According to the equation set (1), the short cycle number C1A and the long cycle number C1B can be worked out during the first frequency division, and in this equation set, M is the sum of the number of short cycle and long cycle; Tclk is the cycle of input clock; Tout is the cycle of objective output clock; TA is the cycle of short-range clock; TB is the cycle of long-range clock; E0A is the error between the cycle value of short-range clock and the cycle value of objective clock after N frequency division ;and E0B is the error between the cycle value of long-range clock and the cycle value of objective clock after N+1 frequency division, so N frequency division and N+1 frequency division can be regarded as the 0th frequency division round.

$$\begin{aligned} \mu_1 &= C_{1A}E_{0A} + C_{1B}E_{0B} \\ C_{1B} &= M - C_{1A} \\ T_{out} &= T_{clk}K \\ T_A &= T_{clk}N \\ T_B &= T_{clk}(N+1) \\ E_{0A} &= T_{out} - T_A \\ E_{0B} &= T_{out} - T_B \end{aligned} \qquad \text{Es(1)}$$

When the number of short cycle and long cycle is being calculated, and provided that μ1=0, which means that the error equals 0, The number of short-range clock and long-range clock can be worked out as decimals, and the parameter must be an integer when Verilog code is being written.

So the integral approximation should be made to C1A and C1B ,which then will be substituted into the above formula to get the actual error. With C1A and C1B as the approximate integral values, the resulting clock actually has certain errors with the objective output clock. This clock can be taken as the long-range clock in dual-modulus decimal frequency division in the next round. After a dual-modulus decimal frequency division is carried out to C1A-1 (the number of short-range clock as -1) and C1B+1 (the number of long-range clock as +1), the resulting output clock is the short-range clock dual-modulus decimal frequency division in the next round.

Above all, the computing method of parameters in "i" rounds of frequency division can be concluded as follows:

1. Let μ1=0 then calculate C1A and C1B.
2. Calculate C2A and C2B according to Es (2).
3. Calculate C3A and C3B according to Es (3).

…

i. Calculate CiA and CiB according to Es (4).

$$E_{1A} = C_{1A}E_{0A} + C_{1B}E_{0B}$$
$$E_{1B} = (C_{1A} - 1)E_{0A} + (C_{1B} + 1)E_{0B}$$
$$\mu_2 = C_{2A}E_{1A} + C_{2B}E_{1B}$$
$$C_{2B} = M - C_{2A} \qquad \text{Es (2)}$$

$$E_{2A} = C_{2A}E_{1A} + C_{2B}E_{1B}$$
$$E_{2B} = (C_{2A} - 1)E_{1A} + (C_{2B} + 1)E_{1B}$$
$$\mu_3 = C_{3A}E_{2A} + C_{3B}E_{2B}$$
$$C_{3B} = M - C_{3A} \qquad \text{Es (3)}$$

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…

…

$$E_{(i-1)A} = C_{(i-1)A}E_{(i-2)A} + C_{(i-1)B}E_{(i-2)B}$$
$$E_{(i-1)B} = (C_{(i-1)A} - 1)E_{(i-2)A} + (C_{(i-1)B} + 1)E_{(i-2)B}$$
$$\mu_i = C_{iA}E_{(i-1)A} + C_{iB}E_{(i-1)B}$$
$$C_{iB} = M - C_{iA} \qquad \text{Es (i)}$$

TABLE I. THE PARAMETER AND ERRORS OF FOUR ROUND

	A	B	C	D（s）	E（s）
R1	M	C1A	C1B	E1A	E1B
R2	M	C2A	C2B	E2A	E2B
R 3	M	C3A	C3B	E3A	E3B
...	…	…	…	…	…
Ri	M	CiA	CiB	EiA	EiB

The calculated parameters are summarized which shown in table I. In table1, A is the total number of cycle; B is the number of long clocks; C is the number of short clocks; D is the error of long clocks; E is the error of short clocks

This decimal frequency divider consists of dual-modulus decimal frequency divisions in an i divide rounds, and output clock will have serious jitter if the N+1 frequency division is made after the N frequency division, so a right way should be found out to uniformly combine the N and N+1 frequency division.For instance, in (3), (4) ,(5) and(6), y is the integral value after dividing CA by CB or the integral value after dividing CB by CA, and R is the remainder after dividing CA by CB

or the remainder after dividing CB by CA.

$$y = \mathrm{int}(\frac{C_A}{C_B}) \quad (3)$$

$$y = \mathrm{int}(\frac{C_B}{C_A}) \quad (4)$$

$$R=CA\%CB \quad (5)$$

$$R=CB\%CA \quad (6)$$

We can insert a long cycle after each y short cycle among M-R cycles, which can effectively reduce the jitter of output clock.

III. SIMULATION

A. Required Parameters

In this paper, the way which is used to test the above frequency division method is a four-round frequency division,. Because after four rounds, the deviation between fin and fout is under 10E-9, with the crystal frequency of 40MHz, output clock frequency of 220.805KHz and frequency dividing ratio of 181.155. The following table II shows the parameters required in every round of frequency.

TABLE II. THE PARAMETER AND ERRORS OF 181.155 FREQUENCY DIVIDER

	A	B	C	D(s)	E(s)
R1	1024	865	159	1.14E-09	-2.39E-08
R2	1024	978	46	1.92E-08	-5.75E-09
R3	1024	236	788	1.09E-08	-1.41E-08
R4	1024	580	444	1.88E-08	-6.19E-09

Higher frequency accuracy would be obtained in each round than that in the last round .When it comes to the fourth round, frequency accuracy could be high enough.

B. The Results and Analysis of Simulation

We put the data on the table above into Verilog-HDL code, and carry out function simulation with MODELSIM 6.5SE with simulation time as 2.1E10ns. Figure 2 and Figure 3 shows the results.

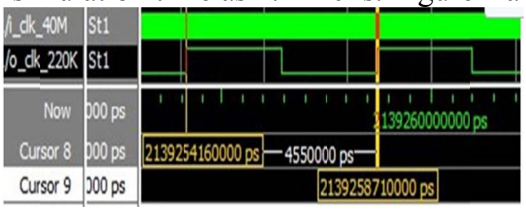


Figure 2: 181 Clock Frequency Divid

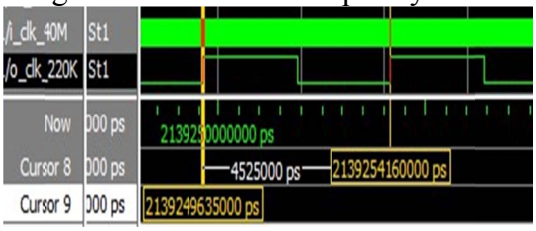


Figure 3: 182 Clock Frequency Divide

In Figure 2 and Figure 3, it can be indicated that the waveform of o_clk_220K output clock composes of two kinds of cycles, as one is 4550000ps and the other is 4525000ps (it is equal to the dividing frequency of i_clk_40M input clock of 181 and 182KHz). Because there are two different cycles of waveform, we finally got the output clock frequency with 181.155KHz in general.

IV. THE COMPARISON WITH DIRECT DIGITAL SYNTHESIZER (DDS) FREQUENCY DIVIDER

A. Dividing principle of Direct Digital Synthesizer

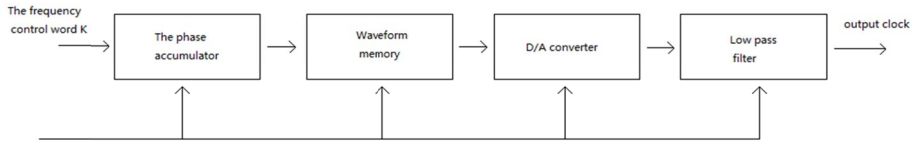


figure 4: schematic diagram of DDS[6]

Figure. 4 Shows the principle of DDS. And a DDS frequency divider composes of phase accumulator, wave memorizer, Digital to Analog Converter (D/A converter) and low-pass filter[5]. The N phase accumulator acquires corresponding phase accumulation code through accumulating frequency tuning word K under the control of CLK. Then the phase accumulation code will converse phase code into range code by the addressing to wave memorizer, which can make it output the different range code. After getting the relevant staircase waveform through D/A converter, finally, the waveform we need will be obtained by low-pass filter.

The output frequency of DDS can be calculated according to the equation (6) [7-8].

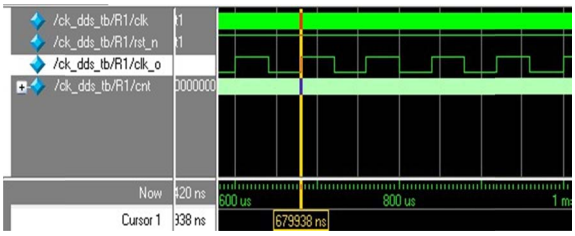
$$f_{out} = K\frac{f_{clk}}{2^N} \qquad (6)$$

In the equation, f_{out} is the output frequency of DDS; K represents the frequency tuning word and N is the bit wide of phase accumulator. According to the equation (6), on the condition that N is a definite value and the value of output frequency is need to change, the value of K is the only one that is needed to change.

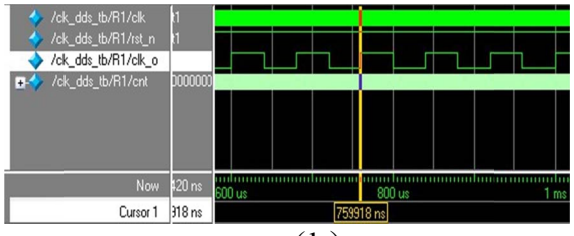
B. Cases of DDS

Assumed that N=32 and the clock frequency is input. If we want the output frequency to be 1KHz, the data can be put into(7), then we will get the result that K ≈ 107400,and when cnt<231，the output clock is 0, or it would be 1.

According to the data above, a DDS frequency divider is designed based on Verilog-HDL code. The following picture is the screenshot of simulation.



（a）



（b）

Figure 5 Simulation Of DDS Divider

C. The Comparison between DDS and High-accuracy Decimal-n Frequency Divider

The main advantage of DDS frequency divider is high frequency resolution, which can achieve fast changing-over of frequency and maintain the continuity of phase. What's more, it is easy for DDS frequency divider to realize numerical control of frequency, phase and range. In addition, it has small volume and low cost. While it's major shortcomings are limited in working frequency and

poor performance in phase noise and stray. Owing to the structure and working principle of DDS, its working frequency would be limited by the velocity of device, which has direct relation with reference frequency.

The decimal frequency divider designed in this paper is an expansion on the basis of dual-modulus prescaler. It applies HDL code to write program so that we can save Phase Locking Loop (PPL) resource of Field Programmable Gate Array (FPGA), which is good in transposability. Therefore, this design can be widely applied to the design of FPGA clock circuit, which can offer the clock source for some modules that require high frequency.

V. CONCLUSION

As a fundamental module, dividers can be widely used in integrated circuit (IC). The design of decimal frequency division can be completed through PPL, but it requires many gate sources and layout areas. Therefore, this method sometimes can't meet the requirements of some designs that need larger layout areas., The decimal frequency divider designed in this paper has modified the basic algorithm according to the traditional dual-modulus prescaler, which can help to control the error range of the final output frequency in a small range, It is a resource-saving decimal frequency divider for circuit designers.

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