Information Acquisition of Laser Tracker Incremental Encoder Based on FPGA

Xiaoyang Wang[1], Yanbing Liang[1], Heng Shi[1] &Weixiang Zhou[1]

[1]Xi'an Institute of Optics and Precision Mechanics of CAS, Xi'an, 710119, China

Keywords: Laser tracker, FPGA, Incremental encoder, Verilog HDL, Logic analyzer

Abstract. Under the laser tracker measurement of angle subsystem environment,signal acquisition system of laser tracker incremental encoder based on FPGA was designed in this paper. The FPGA in this system was mainly responsible for the encoder signal acquisition, processing, and generating timing signals, data caching mechanism and asynchronous output of the data. This paper detailedly introduced quadrupler frequency, phase discrimination, counting, latches, and UART asynchronous serial port output sub-modules in the process of signal acquisition of FPGA, which was implemented by Verilog HDL language. Online logic analyzer of the Quartus software acquired the value of encoder signal in real time, and the rationality of the design was verified ultimately.

Introduction

Laser Tracker System is a kind of high precision industrial measuring system of the large-scale measuring instruments. It involves photoelectric detection technology, laser interferometry technology, computers and control technology, precision machinery, modern numerical methods and other advanced technologies. It has high accuracy, high efficiency, real-time tracking, quick installation, easy operation, and other characteristics for space target tracking and real-time measurement of three-dimensional coordinate space of the target, and it is suitable for the assembling and measurement of large size work-piece. The paper focused on the incremental encoder signal acquisition system in the angle measurement of laser tracker, and detailedly analysed that the encoder played a key role in the data of laser tracker angle measurement. Photoelectric encoder is a sort of sensor, which converts the mechanical geometry displacement of the output shaft into a pulse or digital value. Photoelectric encoder is composed by grating disc and photoelectric detection devices. It is widely used in industrial automatic control field, which can achieve high precision measurement of angular position. Grating disc is divided into some rectangular holes in a circular plate of certain diameter. Since the photoelectric encoder is coaxial with the motor, when the motor rotates, grating disc has the same rotation speed with the motor, and the detection device, which is composed of light-emitting diodes and other electronic components, detectes several pulse output signals, and by calculating the photoelectric encoder output pulses per second the current speed of the motor could be got. Moreover, in order to determine the direction of rotation, encoder also provides two pulse signals, whose phase difference is 90 degrees. According to the methods of its calibration and signal output form, photoelectric encoder can be classified into three categories: incremental encoder, absolute encoder, and mixed encoder. Among them, incremental encoder with high accuracy, high resolution and high reliability is applied in large Laser Tracker measurement devices, and it has played a key role in the angle measurement of laser tracker.

The selection of the encoder

Because the angle error was an important error source of precision laser tracker, so a high request of the encoder's precision was put forward. This system chosed circular grating encoder of Renishaw REXM, which had ultra high precision, its outer diameter was 100mm, a new type DSi interface of Renishaw was used, the two read heads of SiGNUM ™ SR was installed on a REXM ring, which output a reference position signal of propoZ. propoZ had good repeatability, and was completely unaffected by the bearing displacement and power cycle. By DSi combining signals of

the two reading heads together, eccentric was corrected easily. Once DSi eliminated eccentricity, residual error was only the inherent error and the periodic error, two kinds of errors were very small. When REXM and DSi were used cooperatively, the overall installation errors achieved better than 1 second. Circular grating used 5V DC power supply, and the signal output was RS422A serial port. Two angle encoder were used to acquire the value of azimuth and elevation of laser tracker angle values respectively. Circular grating read heads and Renishaw REXM are shown below:

Fig.1: The REXM of Renishaw and its read heads

The principle and design of quadruple circuits

Incremental encoder pulse count module. In order to increase the number of count pulses in a cycle and improve the resolution of measurement, quadruple circuit was designed. Compared with the count circuit composed of discrete components, the quadruple circuit based on FPGA had many advantages,such as lower power consumption, higher stability, better portability, longer component life and so on. Output datas of encoder were firstly stored in the latch, then they were triggered by synchronized control pulse signal, and last output to the module of ARM11. According to the actual data exchange, a certain capacity of FIFO was opened on FPGA as the buffer of data latching, the latch of data exchange was triggered by snchronous control pulses, and in this way the synchronicity and stability of data exchange was ensured. System clock was 10MHz. Synchronization control pulse was divided by system clock, producing 1KHz clock. The system block diagram of FPGA of the part of encoder information acquisition is shown in Figure 2:

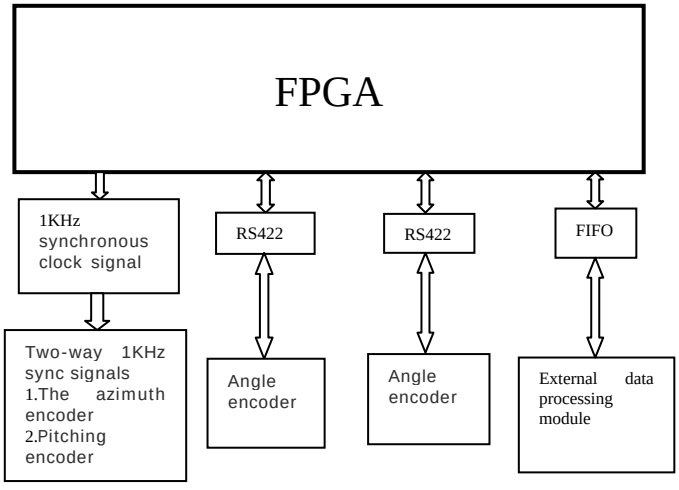

Fig.2: The system block diagram of FPGA

Incremental rotary encoders output A phase, B phase and Z phase output, each of them was the differential signal, the number of signals were six. The signal used TTL level, and the A phase and B phase signals could be conveniently used to judge the direction of rotation encoder. When the encoder was clockwise, A phase signal lead of 90 degrees than B, and when the encoder was reverse, A phase signal lag of 90 degrees than B. Z phase signal was used for zero setting and synchronous control, which sent a reference pulse Z as reference zero at each turn, used to eliminate the cumulative error of laser tracker, so as to improve the accuracy of measurement.

Design of encoder drive module. In the encoder output cycle, A, B phase output signals produced a total of 4 jump edges, at the rising edge and falling edge of signal A and B, the count was conducted respectively, and the revolution of optical-electricity encoder was increased by four times, and in this way fourfold frequency count was realised. The function module used finite state machine (FSM), which was a sequential circuits, and was an important method to implement logical control of high efficiency and reliability. FSM implemented the control of quadruplicated frequency sampling to the original signal, which had higher efficiency. As the driven clock signal of state-machine, the disturbance of jitter was filtered out by an additional high-speed sync signal. A phase and B phase signal state transitions were shown in the figure 3:

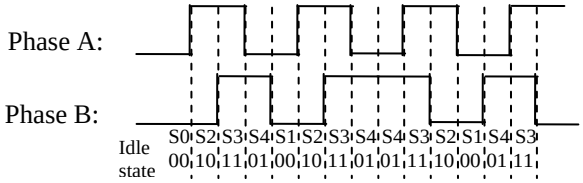

Fig.3: A phase and B phase signals state transitions

Ideally, if the encoder was clockwise, the level value of A and B phase was: 00-10-11-01-00. If the encoder was reverse, the level value of A and B phase was: 00-01-11-10-00. But in practice, because of the jitter and burr in the input pulses , the level state of A phase and B phase would jump effectively in the state machine. When input pulse jitter, the counter can count backwards, so the final count value remains unchanged, the resulting output was not changed, so as to achieve the effect of the de-jitter. Finite state machine had 5 states: IDLE (S0), ALBL (S1), AHBL (S2), AHBH (S3), ALBH (S4). Among them, IDLE was the initial state, which was used for state initialization of counter status.The state-jump of state machine was shown below:

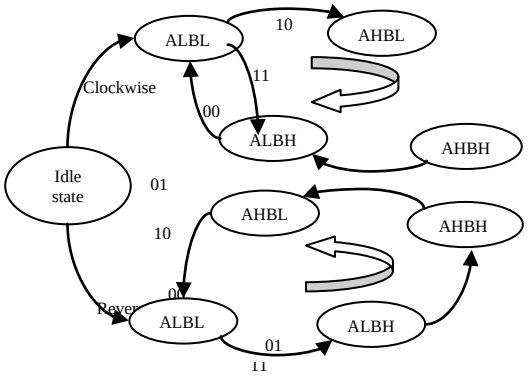

Fig.4: The state-jump of state machine

Implementation of the driving module. Based on the above analysis, when the original signal of encoder output was processed by finite state machines, the four-frequency output signals were obtained. The quadruplicated frequency control and tally function of this system were realised. Compared with quadruple frequency counter circuit consisting of discrete devices, this disign had higher stability, better portability , more flexible, and more stable and reliable.

Due to the incremental encoder without memory function, it was very sensitive to interference caused by external factors. In practical application, because of mechanical vibration, unstable of the working environment, as well as the vibration of motor load, the pulse of encoder would jitter at the edge of a certain pulse phase, and the burr of the signal must be filter out, to improve stability and practicality of the system. D trigger was applied to filter. Trigger was driven by CLK_1KHz clock, and the burr of less than one clock cycle was filtered out by the filter. Register transfer level structure of the filter was shown in the figure 5:

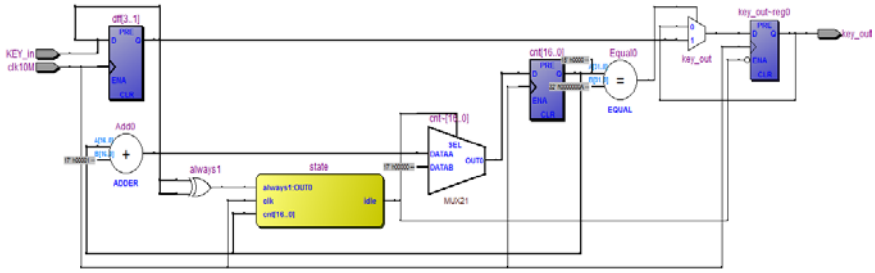

Fig.5: Register transfer level structure of the filter

The design of entire program used a combination of graphics and language methods to achieve top-level module structure diagram was shown in the figure 6:

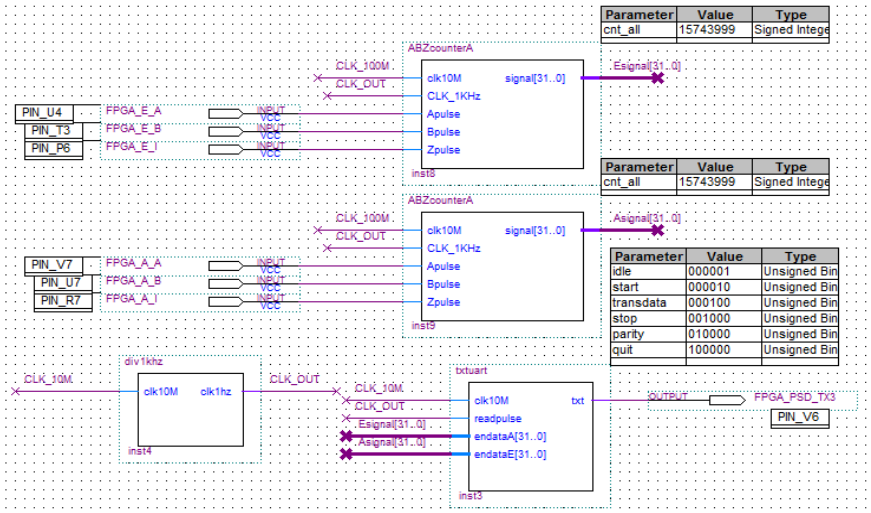

Fig.6:Top-level module structure diagram

The Register Transfer Level of entire design was shown in Figure 7:

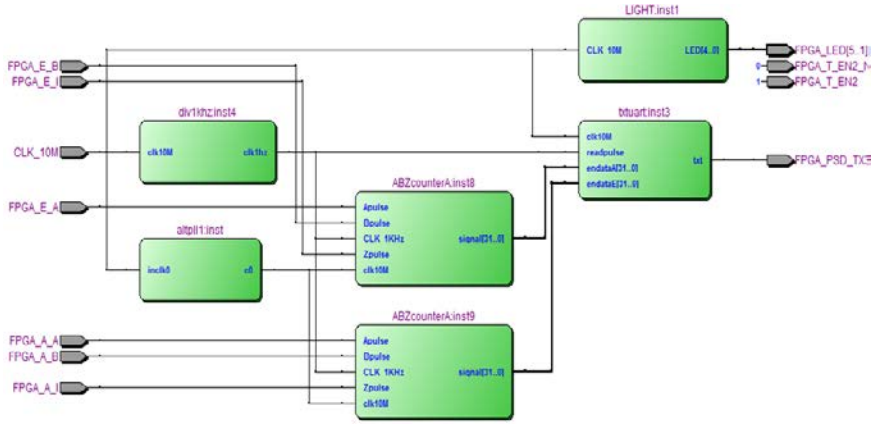

Fig.7: Top-level module structure diagram

The simulation result

The hardware of the system used Altera Stratix II FPGA series of chip EP2S30F48414. The design of state machine was realised by hardware description languages Verilog HDL. And at the same time ,the signal acquisition of encoder, quadruplicated frequency, phase distinguishing, and asynchronous serial output were accomplished. Timing simulation analysis was performed in the Quartus II 10.1 integrated development environment. Simulation diagram of Logic Analyzer as shown in the figure 8:

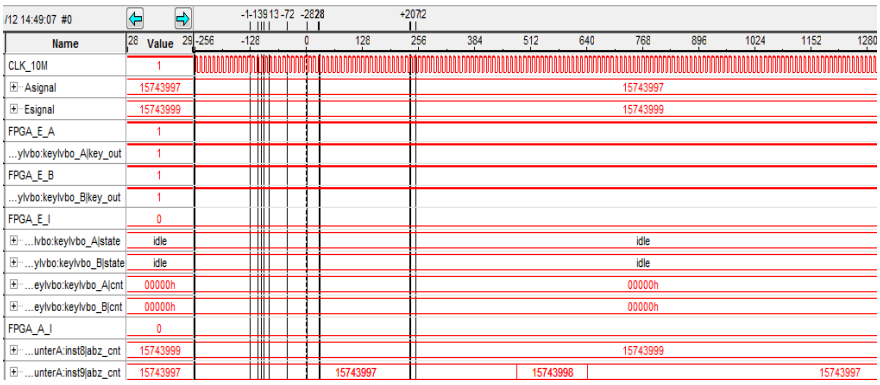

Fig.8: Simulation diagram of Logic Analyzer

According to the angular accuracy and structure size requirements of laser tracker, the outer diameter of circular grating was 100mm as the azimuth axis and elevation axis encoder, whose engraved lines were 15744, and the measurement accuracy is 0.001. The simulation result in figure 8 shows that the incremental photo-electricity encoder successfully completed the function of counting, and the result achieves design requirements.

Conclusions

Laser Tracker angle error is the main source of systematic errors. In order to optimize the angle measurement error, Renishaw REXM was chosed, and the photoelectric encoder quadruple circuit was designed, and the interference and jitter in the process of signal collection were eliminated by filter. The system were designed by Verilog HDL, which was verified by logic analyzer of Quartus 8.1. The information collection integrity of incremental encoder was realised, and ultimately the angular accuracy of laser tracker was guaranteed.

References

[1] Zhou Peisong. Design of Real-time Synchronous Multi-channel Data Acquisition System of Laser Tracker.
[2] Huan Baogui, Lei Bin & Wang Peng. Interface Design and Implementation for FPGA Incremental Encoder.
[3] Chao Jing, Wang Xiaochun & Jiang Hong. Fourfold FrequencyMultiplication C ircuitDesign of Incremental Opto-electric Encoder Based on FPGA.
[4] Lin Jiarui, Zhu Jigui & Zhang Haolin. Field evaluation of laser tracker angle measurement error.
[5] Zhang Shengchao, She Hongbo. Design for Incremental Encoder Interface Circuit Based on FPGA.
[6] Liu Ling. The FPGA implementation of digital signal processing.
[7] Li Zhenghui, Yu Ping. SignalCollection and Processing for Photoelectric Encoder Based on FPGA.
[8] Steve Kilts. Advanced FPGA Design Architecture, Implementation,and Optimization .
[9] LiuWenkui, Shi Jianling. The application of optical rotary encoder in angle measure.
[10] Gan Lin, Li Xiaoxing. Site measuring accuracy testing of laser tracker.