The Design of real-time Image Compressing System Based on DSP and FPGA

Lu Lin [1, a], Li Xiaofeng [1,b]

[1] Beijing Institute of Technology, China

[a] lulin_mail@yeah.net, [b] lixiaofeng@bit.edu.cn

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Abstract. This paper comes up with a high frequency frame real-time image compression technology which is based on high frequency frame camera. On the basis of the technology, I designed a high-frequency frame real-time image processor hardware system that combined TMS320CDM642 with EP2C35 FPGA. Based on TI's DSP / BIOS and the JPEG2000 compression algorithm that supports XDAIS, and used two ping-pong SRAM structures, the system achieved 100 frames per second compression rate. At the same time, the Image Compressing System solved two problems of volume and speed, tested the collecting process and compressing process working simultaneously, and increased the speed of image compression dramatically.

Introduction

At present, most of the input signals of image collecting system are PAL or NTSL CVBS complex signals. PLA is 25 frames per second, and NTSC is 30 frames per second[1,2]. In the industry control, defense and aerospace field, high frequency image collection system can be used to improve accuracy while detecting fast-moving object or observing instant physical phenomena, and Anglicizing data. Aiming at image sensor with Camera Link, I designed a high-frequency image collection system that is 100 frames per second, after compressing the data with JPEG; these data can be transported to monitoring system via RS422.

System Architecture

The system includes Camera Link interface module, the image acquisition pretreatment and transmission module were based on FPGA, the image compression and remote data transmission module was based on DSP[3,5]. Good access memory is necessary for collecting and processing data, but using general SRAM can cut costs. According to its function, it includes collection SRAM and compression SRAM; FPGA controls write and read logic; ping-pong mechanism is used for switching. The whole system structure is shown as follows. Figure 1 showed the structure of the system

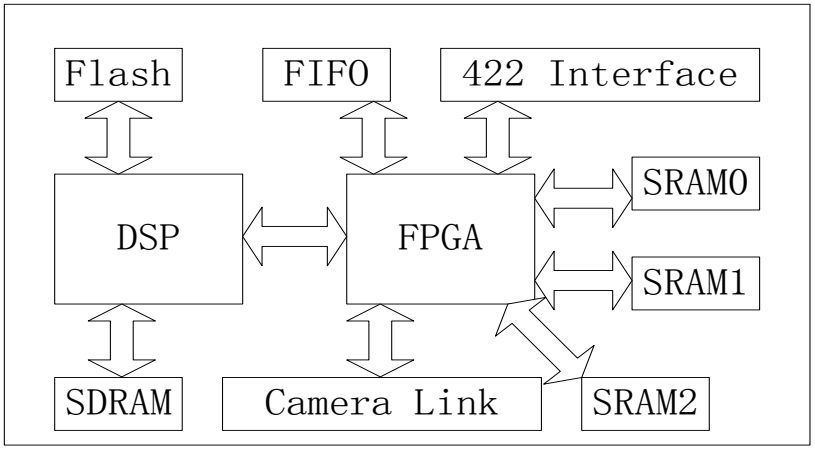

Figure 1 System structure

The system works as this way: the image signal turns into LVTTL via LVDS chips. When a signal crosses a clock domain, it appears to be an asynchronous signal to the circuitry in the new clock domain. The circuit that receives this signal needs to synchronize it. Synchronization prevents the metastable state of the first storage element (flip-flop) in the new clock domain from propagating through the circuit.

FPGA module

The Camera Link interface module. The Camera Link interface module aims at changing LVDS signals that be transferred by high frequency frame digital camera distance.

SRAM Ping-pong cache. The first step for the cache mechanism is S0, the program will produce new data in order to come into the S1, at the same time, it can return to S0 by resting system[6]. When S1 write data to SRAM0, it will reach S2, then S2 will read data from SRAM0 until there is no data in SRAM0. After finishing reading, it will come into S3 for next process. S3 will read data from SRAM1 and check if there is no data in SRAM0. In the whole process, S3,S2 and S1 can return to S0 by resting system. Figure 2 showed the process of cache mechanism.

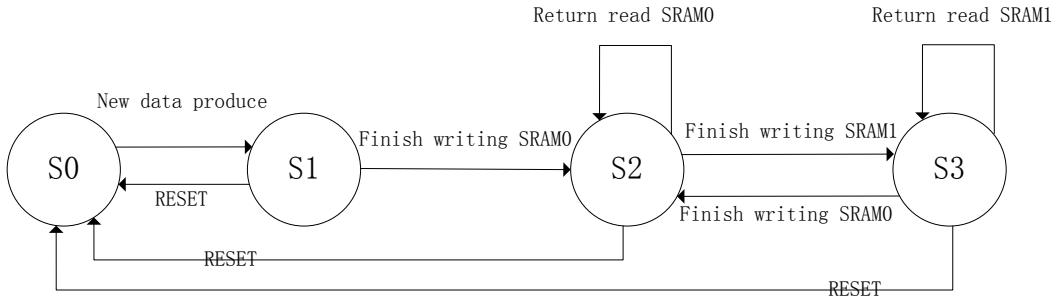

Figure 2 Ping-pong' structure and state transition diagram

SRAM Ping-pong circuit is showed as figure 3. Wr_data is an image data received by Camera Link and it only includes gray scale signal. To manage the image data more conveniently, every pixel and every line of pixel all corresponds to the permanent address of SRAM, so wr_addr is the pixel's address in SRAM; it also means the pixel's address in an image. CHANNEL_SEL will read SRAM flag bit, 0 represents SRAM0, and 1 represents SRAM1.

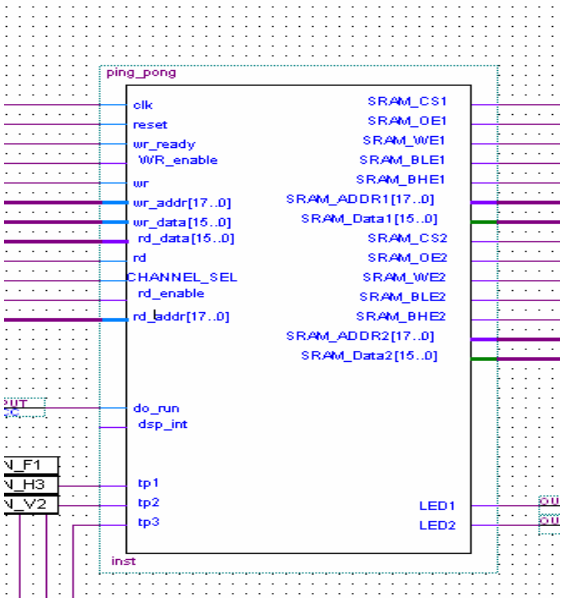

Figure 3 SRAM Ping-pong schematic

FIFO cache module and RS422 transfer module. The TMS320DM642 chip of the TI Company is a high- performance video processor; its dominant frequency can be 600 MHz and its digital processing capacity can be 4800MIPS. The flow chart of DSP program is shown as figure 4. Just after initialize related peripherals and EDMA register, the DSP responds to the interrupt event to send

the EDMA[7]. In the system, EXITUINT4 interrupt rising edge will produce EDMA to transmit. After receive the signals that FPGA sends, EDMA transferring process starts; the whole process nearly costs 10ms. After finish transmitting, EDMA interrupt will be triggered and produce a soft interrupt in service functions which can compressing the image data.

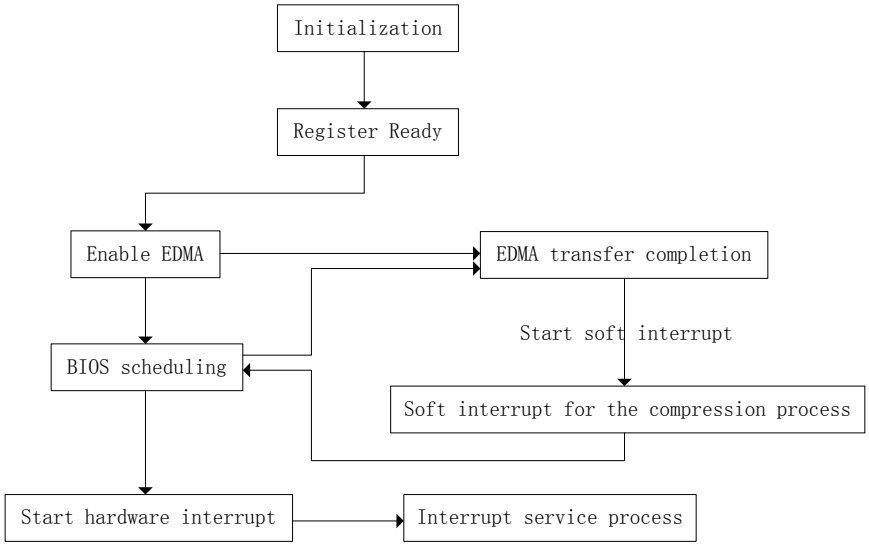

Figure 4 the flow chart of DSP program

The design of DSP/BIOS

If only use EMDA Ping-pong method to send data, it's not enough to achieve that collect and compress data at the same time.. In addition, DSP/BIOS is necessary that it can control in tasks, hardware interrupts, software interrupts, and compress image in soft interrupt service function. The DSP／BIOS of the TI Company is a real-time operating system kernel, and its size can be cut. Depend on the rich kernel service that DSP／BIOS provides, developer could create the application fast.

The design of DSP program

The design of EDMA Ping-pong program. When using the internally generated clock, it may create some functionality and deadline problems. Combinational logic can produce clock that can cause burrs, and create functionality problems， moreover, the delayed happening can lead to deadline problems. The design uses many integer multiples of the global clock to divide the frequency. But due to the integral multiple of the frequency is a little big, if take advantage of DCM in FPGA, it is hard to achieve this goal. In the way of using synchronous counter frequency method, and adding register output before sending every clock signal, it can avoid burrs to be blocked on the register data input sport.

Data switching problems of DSP and FPGS. Due to the compression algorithm adopts JPEG of MECOSO Company, after optimizing and processing, it only takes 4ms to compress an image. So the speed of sending data from EDMA to SDRAM is the key technology to make the system achieve high frequency. In the design, the capacity of the no-frame image is 600x480=288K, and it takes 10ms to send an image. There are two issues to influence the speed; one is ECLOCK that EMIF uses, another is register about EMIF related settings. In the system, ECLOCK uses CPU4 frequency divider of ESP, so the clock of EMIF works at 150MHz, and it increases the speed of sending dramatically. Due to SRAM reflects on the CE2 space of the DSP, thinking about reading data need three steps: set up, strobe and hold. So we set the time of creating CE2 related registers and strobe as one clock, Hold time is 0. In this way, the data throughput of EMIF is:

[EMIF_clock(150MHz)/ Execution cycle(3 clock)]* Bus Width(16bit)=100M/s

Conclusion

Image compressing system taking in this essay achieves video signal input image acquisition that resolution is 600*480 and compression rate is 100 per second, and compresses data with JPEG. The program the system uses is DSP+FPGA, although it is an organizational method, it solved some key problems. The system increases the speed of image compression dramatically, and becomes more flexible. Nowadays, the system applies to monitoring in the space, and it is stable. The inadequacies of this paper are that we did not provide some index to evaluate the performance of the System, and there are no practical applications examples to prove the practicality of the system. So the next work should pay more attention on the performance criteria, and the system will be used in practice.

References

[1] S.KILTS: Advanced FPGA Design: Architecture, Implementation, and Optimization (New Jersey press, Switzerland 2007).
[2] S. S. Junnarkar: Nuclear Science Symposium Conference Record Vol.2 (2005), p. 23-29.
[3] M.D. Fries , J. J.Williams: Nuclear Science Symposium Conference Record Vol.10-16(2010) ,p . 580-584.
[4] D. Wilkinson: Annu. Rev. Nucl. Part. Sci. Vol.45(2004),p.35-39.
[5] P. Allen,D. Holberg :CMOS Analog Circuit Design, Second Edition,(Oxford University Press, New York 2002).
[6] M.A. Green: High Efficiency Silicon Solar Cells (Trans Tech Publications, Switzerland 2005).
[7] J.Q .Wang,G .Jin,C.X .Yang: Optics and Precision Engineering Vol.12(2005),p.105-116.