Graphene Field-effect Transistor Modeling Based on Artificial Neural Network

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Abstract—Simulations and verifications on graphene electronic devices are foundations for application of graphene in integrated circuits. Modeling on graphene metal-oxide-semiconductor field-effect transistor is implemented with artificial neural network. The proposed model has high accuracy and high efficiency. The computational time for the MOSFET model is decreased significantly. More importantly, the novel model for graphene MOSFET is realized in HSPICE software as a subcircuit, which may obviously increase the efficiency of simulations on graphene large scale integrated circuits.

Keywords-graphene; field-effect transistors; modeling; artificial neural network; HSPICE

I. INTRODUCTION

With the rapid development of the semiconductor industry, the feature size of the metal-oxide-semiconductor field-effect transistors (MOSFET) has been scaled down seriously. Traditional silicon transistors may reach their physical limits in next 10 years. A great deal of effort has focused on novel materials to substitute silicon material in preparing transistors [1-3]. Due to the outstanding electrical characteristics of graphene, such as high electron mobility and modulating band gap by changing its width [4], extensive studies on grapheme FETs have been realized and graphene FETs with different device structures are prepared. Top -gated and back-gated graphene FETs have been successfully fabricated recently [5-9]. Channels in these FETs are formed with single-layer or double-layer grapheme [10-12]. More importantly, graphene FET based circuits and blocks, for example frequency multipliers, signal mixers and amplifier have been demonstrated [13-15]. These explorations promote studies on graphene integrated circuits.

Model for the graphene FET is the foundation of predicting performances of designed graphene circuits in different environments. Most early researches on the model of graphene FET are realized with the non-equilibrium Green's function method [16-19]. In these studies, the current-voltage (I-V) characteristics for the graphene FETs in special device structure are calculated. However, these calculations consume a lot of time and the obtained I-V characteristics can't be applied to simulate the performances of graphene FETs. Based on the measured I-V characteristics, physical models for graphene FETs are developed [20-24]. Although detailed physical models have high accuracy in simulations, one limitation of these models is the excessive demanding from a computational point of view. Artificial neural network (ANN) is a powerful tool to simulate nonlinear systems. Especially, ANN has been successfully applied to simulation carbon nanotube (CNT) FETs and nanoscale CMOS circuits [25, 26].

In this paper, model for top-gate graphene FET is put forward based on the artificial neural network. The proposed model has a high accuracy and the advantage of low time consuming. Finally, the model for the graphene FET is realized in HSPICE package as a subcircuit. These explorations may promote studies on the graphene integrated circuits.

II. MODEL AND METHOD

A. Model for I-V characteristics of graphene FET

Duo to the compatibility in fabrications of top-gated graphene FETs and the existing traditional silicon CMOS technology, preparations of graphene FETs in this structure have attracted extensive studies. The schematic diagram of a typical top-gate graphene FET is present in

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Fig .1 (a), in which the channel is formed by single-layer graphene. In essence, the graphene FET is a voltage controlled current source and can be modeled by the circuit in Fig .1 (b). In this model, V_{CH} is the potential of the channel, I_{DS} indicates the current follows through the channel, capacitors $C_{CH,S}$, $C_{SUB,CH}$, $C_{CH,G}$ and $C_{CH,D}$ are used to model the transient current from the charging and discharging of the channel.

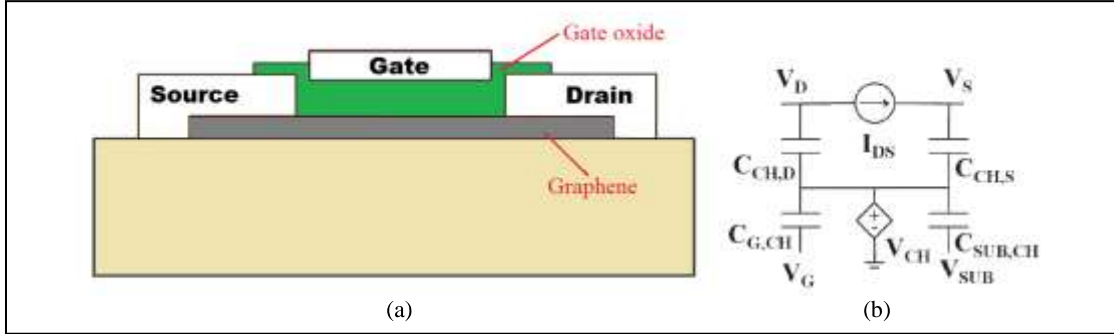

Figure 1. Schematic diagram of top-gated graphene FET (a) and circuit model (b).

Q_{CH} and Q_{CAP} are the channel charge and the charge across all capacitors coupled to the channel. The two charges are functions of channel potential ψ_{CH} and their magnitudes are equal. By equating Q_{CH} and Q_{CAP}, ψ_{CH} can be obtained. Based on this assumption, Jie Deng *et al* developed a novel method to calculate the channel potential, which is adopted in our studies [27]. Channel charge of the FET can be calculated as

$$n_{\alpha} = \int_{0}^{\infty} f(E) D_{\alpha}(E) dE \tag{1}$$

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}} \tag{2}$$

where n_α is the electron in subband ε_α, $D_\alpha(E)$ is the density of states (DOS) of the graphene. $f(E)$ is the Fermi-Dirac distribution function and can be calculated by (2), in which E_F is Fermi energy and k is Boltzmann's constant.

Based on the Landauer-Buttiker formalism, the electron current is defined as

$$I_e(\Psi_{CH}, V_D, V_S) = \frac{2qkT}{h} \sum_{\alpha} [\ln(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}) - \ln(1 + e^{\frac{q(\Psi_{CH} - V_D) - \varepsilon_\alpha}{kT}})] \tag{3}$$

where V_D and V_S are the potentials for the drain and source of the graphene FET. In a N-type graphene FET I_D=I_e, while for a P-type FET, I_D = I_h, which can be calculated in the same method. Cheng et al developed a graphene FET HSPICE model package [28], which is used to simulate the I-V characteristics of the top-gated graphene FET.

B. Neural network computations

Due to powerful self-learning and self-adapting abilities, effective online adaptation and good noise rejection capabilities, artificial neural networks have been widely used in pattern recognition, cluster analysis, signal classification, nonlinear function fitting, etc. [29]. Back propagation (BP) neural network is one of the most widely used neural networks, which is realized with multi-layer perceptron (MLP) composed of numerous

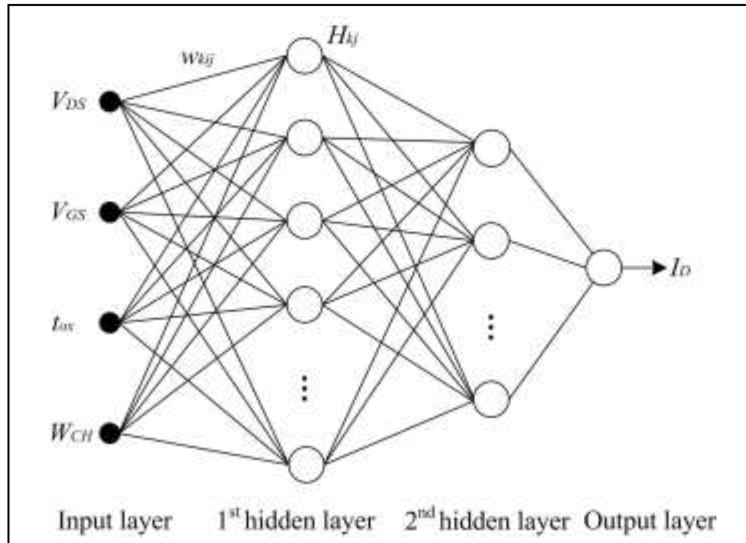

Figure 2. Schematic diagram of BP neural network with two hidden layers.

interconnected neurons. A diagram of a BP neural network with two hidden layers is shown in Fig .2.

Neurons are basic processing elements in a BP network and connected to each other through a set of weights. In the training of the neural network, weights are adjusted based on an error-minimization method. The neural network in Fig .2 consists of four layers named as input layer, the first hidden layer, the second hidden layer and output layer. The output of neuron *j* in hidden layer *k* can be calculated as

$$H_{kj} = f(\sum_{i=1}^{h} w_{kij} X_{ki} + a_{kj}) \qquad \begin{cases} j = 1, 2, \ldots, m \\ k = 1, 2 \end{cases} \tag{4}$$

Where *f* is the transfer function of hidden layer *k*, *w* is the weight, *a* is the threshold and *m* is the number of neurons in the hidden layer *k*. X_{1i} is the input of the network, and X_{2i} is the output of the first hidden layer, which is the input of the second hidden layer.

Tan-sigmoid transfer function is adopted in the two hidden layers, which has been successfully applied in simulations on the I-V characteristics of carbon nanotube FETs [25, 29, 30]. The transfer function is given by

$$f(x) = \frac{e^{x} - e^{-x}}{e^{x} + e^{-x}} \tag{5}$$

where *x* is $\sum_{i=1}^{h} w_{kij} X_{ki} + a_{kj}$ in (4).

The output of the neural network is

$$I_D = \sum_{j=1}^{m} H_{kj} w_j + b \tag{6}$$

where H_{kj} is the output of neuron in the second hidden layer and *b* is threshold of the output layer.

The drain current I_D of a graphene FET is determined by the drain-source voltage V_{DS}, the gate-source voltage V_{GS}, gate oxide thickness t_{ox} and the channel width W_{CH}. The I-V characteristics of the graphene FET are simulated with BP neural network, in which the drain current I_D is the single output and above four parameters determining the drain current are inputs.

III. RESULTS AND ANALYSIS

To train the neural network, about 7700 data for simulation on the I-V characteristics of the graphene FET are obtained using the HSPICE model developed by Cheng *et al*. Ranges for the inputs and output of the simulation are presented in TABLE I.

TABLE I. DATA RANGES THE I-V CHARACTERISTICS OF GRAPHENE FET

Range	Input				Output/μA
	V_{DS} /V	V_{GS}/V	t_{ox}/nm	W_{CH}/nm	
min	0.0	0.0	0.5	0.87	0.0
max	0.5	0.5	2.5	6.36	19.51

In the 7700 data for simulating the I-V characteristics of the graphene FET, about 6700 data are selected as training samples and the remaining are testing samples. To achieve appropriate neural network for simulating the graphene FET, neural networks with structure are tested and optimized, which are realized with MATLAB 2011b. Pearson's correlation coefficients between the testing samples and the predicted values from the neural network are calculated to evaluate the trained networks. Correlation coefficients for five typical neural networks are list in TABLE II. The network 4-11-9-1 has the highest correlation coefficient, which is suitable to simulate the characteristics of the graphene FET.

TABLE II. CORRELATION COEFFICIENTS FOR DIFFERENT NEURAL NETWORKS

Networks	4-9-8-1	4-7-5-1	4-11-9-1	4-7-4-7-1	4-5-5-5-1
Coefficients	0.99965	0.99964	0.99997	0.99963	0.99962

From the family of i_D versus v_{DS} curves (in Fig .3 (a)) of the n-channel graphene FET with a channel width (W_{CH}) of 1.60 nm and a gate oxide thickness (t_{ox}) of 0.95 nm, it can be seen that the maximum error between the prediction of the neural network and result from the analytical model is about 0.076 μA, which is about 0.0039% of the analytical model. All relative errors in the transferring properties between the predictions of the neural network and results from the analytical model of the n-channel graphene FET are smaller than 0.0065%. Prediction values of the 4-11-9-1 neural network are suitable to simulate the I-V characteristics of the graphene FET. Similar results for p-channel graphene FET can also be obtained.

The proposed neural network model can be realized as a subcircuit in HSPICE package. In essence, the graphene FET is a voltage controlled current source. As the current between gate and source is very small and always neglected, a null current source is used to realize this approximation. The drain current can be calculated with the neural network. The general syntax for the subcircuit to simulate the graphene FET in HSPICE package is

```
.SUBCKT GrapheneFET Drain Gate Source
iGate Gate Source 0
iDrain Drain Source current='Drain current calculated by the neural network'
.ENDS
```

where "GrapheneFET" is the name of the subcircuit. "Drain", "Gate" and "Source" are the electrodes of drain, gate and source for the graphene FET.

In order to validate the proposed neural network model, an inverter formed with n-channel and p-channel graphene FETs is designed. The outputs of the inverter from the analytical model and neural network model are plotted Fig .4. By comparing the outputs from the two models, it can be seen that a high similarity is achieved and the neural network model is suitable to simulate the performances of graphene circuits. It is well known that the neural network has a high efficiency in simulations on nonlinear systems. CPU time consumptions for simulations on the graphene inverter with above methods are listed in TABLE III, which are realized on a computer with an Intel I3 530 CPU and 8GB memory.

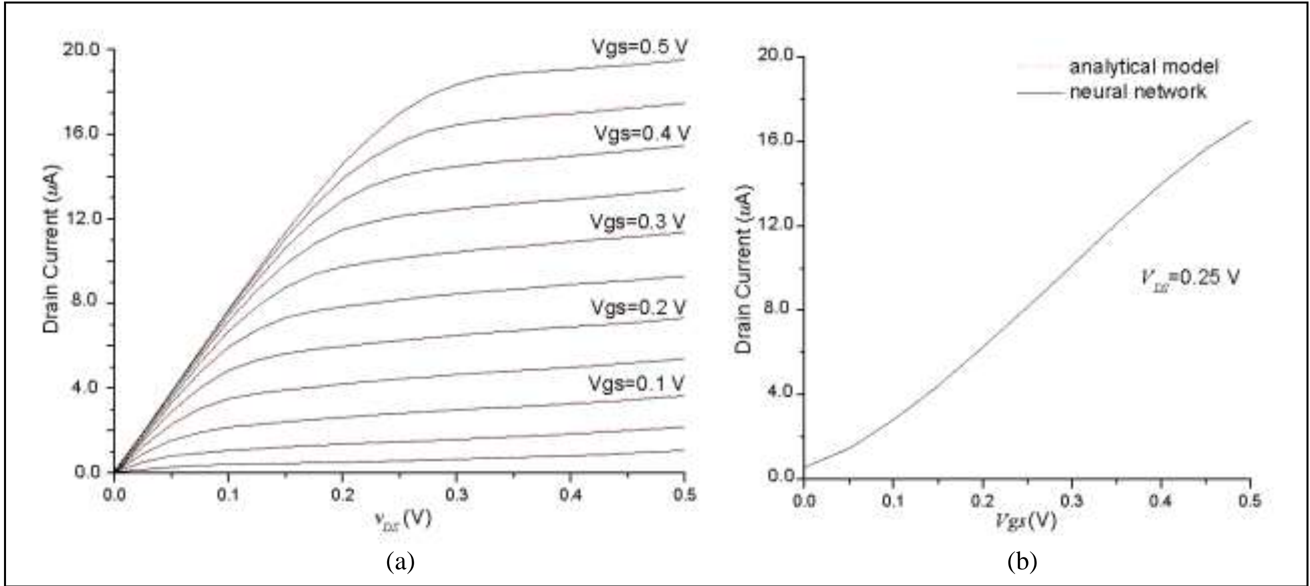

Figure 3. I-V characteristics of an n-channel graphene FET, (a) and (b) are family of i_D versus v_{DS} curves and transferring properties. Red dash line indicates data from the analytical model provided by Cheng *et al* and solid black line means by prediction of the neural network.

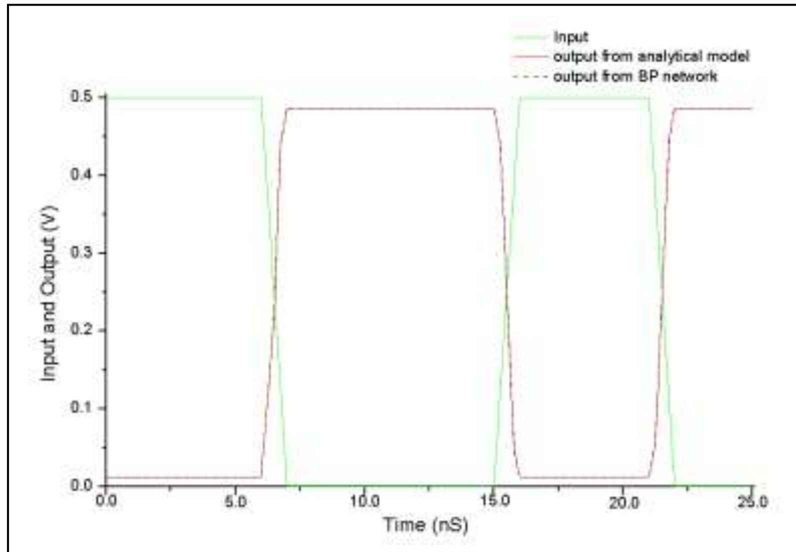

Figure 4. Input and output of inverter based on graphene FET. Red line indicates output from the analytical model put forward by Cheng et al and black dash line means output of the inverter of the neural network.

TABLE III. CPU TIME CONSUMPTIONS FOR SIMULATIONS ON THE OUTPUT OF THE GRAPHENE INVERTER

Method	analytical model	neural network
CPU time /S	7.00	4.62

Compared with the analytical model, the proposed neural network model has a higher efficiency, which saves about 34% time of the traditional analytical model. This advantage may be more significant in large scale integrated circuit simulations. More importantly, the inputs of our proposed model can be extended to include other parameters of the graphene FET, such as temperature and the number of graphene.

IV. CONCLUSIONS

The possibility of applying artificial neural network to modeling the I-V characteristics of the graphene FET is investigated. Data for training and optimizing the neural network are obtained from a traditional analytical model. Errors in the I-V characteristics of the FET between the analytical model and neural network are smaller than 0.0065%. The method to realize the neural network model is proposed and the performances of an inverter based on proposed model are implemented. The advantage of high efficiency for the neural network model is verified. Results in this paper may provide meaningful information on the simulation and verification for graphene integrated circuits.

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