Optimization of Teaching Content of Digital Logic Course Using Hardware Description Languages

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Abstract. With the advent of the artificial intelligence era, the teaching content of Digital Logic course in most universities has not been optimized accordingly, which limits the cultivation of students' practical and innovative abilities to some extent. Therefore, it is difficult to provide effective support for subsequent core courses. To solve the above problem, we propose an optimization plan for Digital Logic course using hard description languages to enhance students' practical and innovative abilities. It mainly includes two aspects: theoretical teaching and experimental teaching. In theoretical teaching, strengthen the contents of programmable logic devices and hardware description languages. The theoretical teaching content is divided into three major parts: the fundamentals of logical algebra, combinational logic circuits, and sequential logic circuits. In the three major parts, sequentially add the introduction of hardware description languages and the design of combinational logic circuits and sequential logic circuits with hardware description languages. On this basis, the experimental teaching content mainly includes design experiments and comprehensive experiments. Students need to use hardware description languages on the Electronic Design Automation (EDA) software platform to complete experiments and write experimental reports. Furthermore, adopt a blended online and offline teaching mode, and integrate hardware description languages into various aspects of theoretical teaching and experimental teaching. In this way, it enhances students' practical and innovative abilities.

Keywords: Digital Logic, Hardware Description Language, Programmable Logic Device.

1 Introduction

The course of Digital Logic is an important foundational course in majors such as computer science and artificial intelligence. As the core course group credits account for a relatively high proportion in the training programs of those majors, the course hours of Digital Logic have been significantly reduced. Currently, in most domestic universities they simply cut some less important chapters based on the course of Digital Circuits in majors such as electronic information engineering and communication engineering to alleviate the problem of limited course hours, but do not optimize the course teaching

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content accordingly with the advent of the artificial intelligence era, which limits the cultivation of students' practical and innovative abilities to some extent. In this way, it is difficult to provide effective support for subsequent core courses. With the development of the Electronic Design Automation (EDA) technology, it has become a trend to introduce the Hardware Description Languages (HDL) such as the Very High Speed Integrated Circuit HDL (VHDL) [1] and the Verilog HDL [2] in the course of Digital Logic [3-4].

In recent years, more and more scholars have introduced hardware description languages into the teaching of Digital Logic. Long et al. [5] used the Field Programmable Gate Array (FPGA) as a tool to integrate the HDL and digital logic courses, and achieved good teaching results. Qi et al. Liu et al. [6] introduced HDL and Logisim/Modelsim simulation software to improve students' abilities of analysis and design. Luan [7] applied FPGA technology in the teaching process of digital logic courses to visualize abstract theoretical knowledge, reduce students' learning difficulty, and cultivate students' practical abilities and innovative thinking abilities. Yang et al. [8] proposed a hybrid teaching mode of digital logic and the VHDL courses, which improved the teaching quality and teaching efficiency. Wei et al. [9] introduced the FPGA experiment platform to put forward the idea of digital logic course construction based on system capability cultivation. Lu et al. [10] asked students to independently learn EDA software online and offline to improve their engineering practice abilities in the process of digital logic experiment teaching.

In short, the traditional method of building digital circuits on digital circuit experimental boxes for experimental teaching is not very suitable for the training objectives of those majors such as computer science and artificial intelligence. Hence, we optimize the teaching content of Digital Logic course by integrating the hardware description language into various aspects of course theoretical teaching and experimental teaching to improve students' practical and innovative abilities.

2 Main Idea

Digital Logic is an important foundational course, which mainly consists of theoretical teaching and experimental teaching. In theoretical teaching, students can study the fundamentals of logical algebra, combinational logic circuits and sequential logic circuits, thus possessing the basic abilities to design and simulate digital logic circuits using small and medium-sized integrated logic devices. In order to further enhance students' innovative practical abilities, strengthen the contents of programmable logic devices and hardware description languages in theoretical teaching, and students use hardware description languages on the EDA software platform to complete experiments in experimental teaching mainly including design experiments and comprehensive experiments. The intrinsic relationship between theoretical teaching and experimental teaching is shown in Fig. 1.

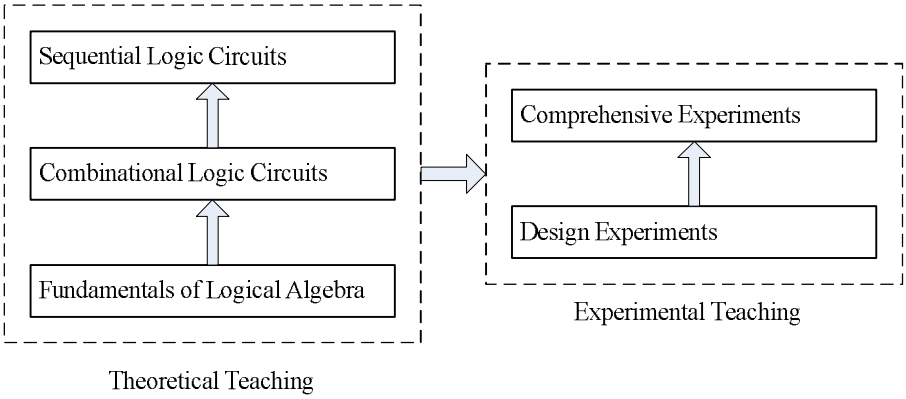

Fig. 1. The intrinsic relationship between theoretical teaching and experimental teaching.

3 Optimization of Theoretical Teaching Content

In order to optimize the theoretical teaching content (see Table 1) of Digital Logic, we reduce the content related to chip internal circuit, strengthen the content related to programmable logic devices and hardware description languages to improve students' students' practical and innovative abilities.

Table 1. The theoretical teaching content.

Chapter	Teaching content
1. Fundamentals of logic algebra	1.1 Overview
	1.2 Three basic operations in logic algebra
	1.3 Basic and common formulas of logic algebra
	1.4 Fundamental theorems of logical algebra
	1.5 Logical function and its description method
	1.6 Simplification of logical functions
	1.7 Logical functions with independent terms and their simplification
	1.8 Introduction of hardware description languages
2. Combinatorial logic circuits	2.1 Overview
	2.2 Analysis method of combinatorial logic circuits
	2.3 The basic design method of combinatorial logic circuits
	2.4 Several commonly used combinational logic circuit modules
	2.5 Design of combinational logic circuits with hardware description languages
3. Sequential logic circuits	3.1 Overview
	3.2 Analysis method of sequential logic circuits
	3.3 Several commonly used sequential logic circuits
	3.4 Design method of sequential logic circuits
	3.5 Design of sequential logic circuits with hardware description languages

3.1 Fundamentals of Logic Algebra

In Chapter 1, on the basis of systematically explaining the basic laws and formulas of logical algebra, introduce hardware description languages in "1.8 Introduction of hardware description languages". And through practical examples such as "three-person voter", students will master the basic grammar of hardware description languages.

3.2 Combinatorial Logic Circuits

In Chapter 2, on the basis of systematically explaining the basic analysis and design methods of combinatorial logic circuits, focus on how to realize MSI devices such as 3-8 line decoder/demux 74LS138 and 1-of-8 line data selector/multiplexer 74LS151 using hardware description languages in "2.5 Design of combinational logic circuits with hardware description languages".

3.3 Sequential Logic Circuits

In Chapter 3, on the basis of systematically explaining the basic analysis and design methods of sequential logic circuits, focus on how to realize the Medium Scale Integration (MSI) devices such as synchronous 4-bit counter 74LS160/161 and 4-bit bidirectional shift register 74LS194 using hardware description languages in "3.5 Design of sequential logic circuits with hardware description languages".

4 Optimization of Experimental Teaching Content

In order to further enhance students' innovative practical abilities, we optimize the experimental teaching content (see Table 2) using hardware description language to program on the EDA software platform to replace the traditional method building digital circuits on the experimental box.

Table 2. The experimental teaching content.

No.	Title	Type
1	Decoder	Design experiment
2	Multiplexer	Design experiment
3	Voter	Design experiment
4	Counter	Design experiment
5	Sequential signal detector	Design experiment
6	Sequential signal generator	Design experiment
7	Digital clock	Comprehensive experiment
8	Password lock	Comprehensive experiment
9	Traffic light controller	Comprehensive experiment
10	Digital frequency meter	Comprehensive experiment

4.1 Design Experiment

There are 6 design experiments in the list of Table 2 such as decoder, multiplexer, voter, counter, sequential signal detector and sequential signal generator. Decoder, multiplexer and voter are combinational logic circuits, and can be directly programmed using HDL or implemented using the components 74LS138 and 74LS151 mentioned in “3.2 Combinatorial logic circuits”. Counter, sequential signal detector and sequential signal generator are sequential logic circuits, and can be directly programmed using HDL or implemented using the components 74LS160/161 or 74LS194.

4.2 Comprehensive Experiment

There are 4 comprehensive experiments in the list of Table 2 such as multifunctional digital clock, combination lock, traffic light controller and digital frequency meter. Their experimental contents are as follows:

1. Title: multifunctional digital clock

Experimental content: Design a multifunctional digital clock. Requirements: Display format is "hour-minute-second". The hourly time is 10 seconds, starting from 10 seconds before the hour. The horn starts to sound until after the hour, and the LED starts flashing 5 seconds before the hour. After the hour, it stops flashing.

2. Title: password lock

Experimental content: Design a password lock. Requirements: The unlocking password must be at least 4 digits (or more) for a password lock. When the input code of the unlock button switch (which can be set to 8 or more positions, only 4 of which are valid, and the rest are dummy) is equal to the set password, the unlock control circuit is activated, and use the green light on and the red light off to indicate the unlock status. If the lock cannot be opened within 5 seconds after the first button is pressed, the circuit will automatically reset and issue an alarm signal. At the same time, use the green light off and the red light on to indicate the locked state.

3. Title: traffic light controller

Experimental content: Design a traffic light controller. Requirements: It displays traffic lights using either the traffic light module from the experimental box or any two of the seven segment code tubes. The system clock selects the 1KHz clock of the clock module, and the requirement for the yellow light flashing clock is 2Hz. The time displayed on the seven-segment code tube is a 1Hz pulse, which decreases every 1 second. When the display time is less than 3 seconds, the yellow light in the direction of traffic flashes at a frequency of 2Hz.

4. Title: digital frequency meter

Experimental content: Design a digital frequency meter. Requirements: The system clock is selected from the 50MHz clock on the core board, with a gate time of 1s (obtained by dividing the system clock). During the period when the gate is at a high level, count the input frequency. When the gate becomes low, record the current frequency value and reset the frequency counter to zero. The frequency display refreshes every 2 seconds.

5 Conclusions

In order to improve students' practical innovation abilities, we optimize the course teaching content by integrating the hardware description languages into all aspects of theoretical teaching and experimental teaching. Especially, abandon the traditional way of completing experimental teaching on the digital circuit experiment box, adopt large-scale programmable logic devices such as FPGA, and carry out experimental teaching through hardware description language programming to improve students' practical innovation abilities.

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