FinFET Technology based Low Power SRAM Cell Design for Embedded Memory

Jami Venkata Suman[1*], Mamidipaka Hema[2], A.Swetha Priya[3], D.Raja Ramesh[4], Patna Syamala Devi[5], and Subba Rao Polamuri[6]

[1]Assistant Professor, ECE Department
GMR Institute of Technology, Rajam, India
Corresponding author: venkatasuman.j@gmrit.edu.in

[2]Assistant Professor, ECE Department
JNTUGVCEV, Vizianagaram, Andhra Pradesh, India
mhema.ece@jntugvcev.edu.in

[3] Research Scholar, ECE Department
Amrita School of Engineering, Amrita Vishwa Vidhyapeetham, Bangalore
a_swetha@blr.amrita.edu

[4] Associate Professor, ECE Department
MVGR College of Engineering (A), Chintalavalasa, Vizianagaram, India
rajaramesh@mvgrce.edu.in

[5]Assistant Professor, ECE Department
Annamacharya Institute of Technology and Sciences, Rajampet, Andhra Pradesh
syamuvlsi@gmail.com

[6] Professor, Department of CSE
BVC Engineering College, Odalarevu, India
psr.subbu546@gmail.com

Abstract. Computer systems rely heavily on cache memory because it offers a quicker and more effective means of accessing frequently used data. It serves as a buffer between the CPU (central processing unit) and main memory (RAM). Electronic devices' energy use during standby or idle mode is referred to as standby leakage, standby power consumption, or vampire power. This is a significant concern because it results in unnecessary energy wastage and can contribute to higher electricity bills and increased environmental impact. Low-energy techniques are crucial in minimizing current leakage and improving the energy efficiency of electronic devices. Current leakage, also known as leakage current or sub threshold leakage, refers to the unintended flow of current in transistors and other components even when they are in an off or standby state. This leakage current can contribute significantly to power consumption and reduce the overall energy efficiency of devices. Designing a 6T SRAM cell using FinFET technology at the 18nm process node involves creating a layout and optimizing the circuit for performance and efficiency.6T SRAM cell using FinFET technology at the 18nm process node requires a deep understanding of circuit design, layout techniques, and semiconductor physics. The goal is to achieve a balance between performance, stability, power consumption, and manufacturability to create an efficient and reliable memory cell. FinFETs offer

K. R. Madhavi et al. (eds.), *Proceedings of the International Conference on Computational Innovations and Emerging Trends (ICCIET 2024)*, Advances in Computer Science Research 112,
https://doi.org/10.2991/978-94-6463-471-6_106

improved gate control, reduced leakage current, enhanced performance, and better power efficiency compared to traditional planar transistors. These features make FinFET technology a electronic cornerstone of modern semiconductor design, enabling the development of high-performance, energy-efficient devices.

Keywords: 6T SRAM, Cadence Virtuoso; MOSFET, Efficiency, Standby leakage current, FinFET.

1 Introduction

SRAM, or Static RAM, is a type of volatile memory. İt is used in computers and digital electronic devices. It is often used as cache memory in CPUs and as on-chip memory in digital circuits due to its high-speed access and ability to retain data without constant refreshing. It is faster than dynamic RAM (DRAM) due to its simple memory cell design and lack of the need for refreshing. SRAM is stable, meaning it can hold data as long as power is supplied to it [1-2]. This is in contrast to DRAM, which requires constant refreshing to retain data. An SRAM cell typically consists of 6 transistors arranged in a flip-flop configuration. This structure provides the ability to store a single bit of data.

SRAM offers low read and write latencies, making it suitable for applications where fast access to data is crucial. SRAM is commonly used as cache memory in CPUs to provide fast access to frequently used data. L1, L2, and L3 caches in modern processors are often made of SRAM. SRAM requires more power than DRAM due to its more complex cell structure and constant power consumption [3]. This is a trade-off for its speed and stability. SRAM cell designs require more transistors per bit of data compared to DRAM cells, making it less dense for large memory capacities. SRAM is used in applications where speed and low latency are critical, such as CPU caches, high-performance networking equipment, and real-time systems.

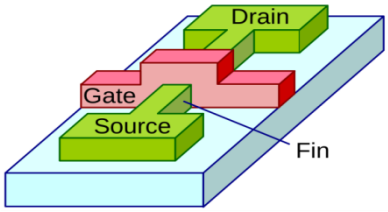

Fig. 1. FinFET design

Fin Field-Effect Transistor (FinFET) is a type of transistor architecture shown in the figure 1 that has become prominent in semiconductor manufacturing due to its ability to address several challenges posed by traditional planar transistors as they continue to scale down in size. FinFET technology offers improved performance, reduced leakage current, and better control over transistor behavior. The FinFET transistor gets its name from its unique fin-like structure [4]. In a FinFET, the channel through which current flows is a vertical fin that protrudes from the substrate, rather than lying flat on the substrate like in planar transistors. This design provides better gate control

and helps mitigate short-channel effects that can cause performance degradation as transistors shrink. The key components of a FinFET include Source and Drain regions control the flow of current between them through the channel [5]. The gate controls the flow of current between the source and drain by modulating the conductivity of the channel.

Advantages of FinFET Technology are Reduced Leakage Current is One of the primary challenges as transistors shrink is increased leakage current, where some current flows even when the transistor is in the off state. FinFETs mitigate this by using the vertical fin structure, which improves gate control and reduces subthreshold leakage. Improved Gate Control with fin structure allows better control over the gate, resulting in improved on-off switching characteristics and reduced short-channel effects. This leads to better performance and stability [6]. FinFETs can operate at lower supply voltages while maintaining performance, which contributes to lower power consumption and energy efficiency. Due to the improved gate control and reduced capacitance, FinFETs switch on and off faster than planar transistors, resulting in better overall performance.

2 Motivation Towards FinFET Technology

A MOSFET (Metal Oxide Semiconductor FET) is a type of semiconductor device used to amplify or switch electronic signals in electronic devices and integrated circuits. It's a fundamental building block in modern electronics and plays a critical role in digital circuits, analog circuits, and power electronics. MOSFET technology is widely used due to its versatility, low power consumption, and ability to operate at high frequencies. MOSFET technology has been fundamental to modern electronics and computing, it also comes with several drawbacks and challenges [7-9]. Leakage Current experience leakage current even when they are in an off state. Gate leakage, sub threshold leakage, and drain-induced barrier lowering contribute to power consumption and reduce energy efficiency. As MOSFETs become smaller and more densely packed, heat dissipation becomes a significant challenge. High power densities in small areas can lead to localized overheating, reducing device reliability and performance. As transistor sizes decrease, short-channel effects become more pronounced [10]. These effects, such as drain-induced barrier lowering and sub threshold slope degradation, can impact the accuracy of transistor behavior and overall circuit performance. In advanced semiconductor processes, variations in threshold voltage due to manufacturing and process variability can lead to inconsistent device behavior and impact circuit reliability.

Gate Oxide Leakage used in small MOSFETs are susceptible to gate oxide breakdown, leading to increased leakage and potential device failure. MOSFETs consume power when transitioning between on and off states. As MOSFETs shrink to smaller process nodes, quantum mechanical effects such as tunneling start to become more pronounced, challenging the continued scaling of these devices. Advanced MOSFET technologies, especially at smaller process nodes, require complex manufacturing processes that are costly and technologically challenging. The

decreasing size of MOSFETs makes them more susceptible to process variations, which can lead to unpredictable and inconsistent device behavior, impacting overall circuit reliability.

As transistor sizes decrease, electromagnetic interference (EMI) and crosstalk between adjacent components become more problematic, affecting signal integrity. Gate-Induced Drain Leakage (GIDL) is a phenomenon where a reverse-biased gate-drain voltage can induce leakage current, impacting power efficiency. Designing high-performance circuits with smaller MOSFETs requires intricate design techniques to manage power consumption, thermal effects, and overall performance [11-12]. As transistor sizes approach the atomic scale, quantum mechanical effects such as quantum tunneling can lead to unconventional behaviors and challenges in maintaining reliable transistor operation. MOSFET technology has enabled the incredible advancements in electronics and computing, it is not without its challenges. Many of these drawbacks become more prominent as devices continue to shrink and as technology advances to smaller process nodes. Researchers and engineers are continuously working to address these issues and develop alternative transistor architectures to overcome the drawbacks of traditional MOSFETs.

FinFET technology offers several advantages over traditional planar MOSFET technology as semiconductor devices continue to scale down in size. Reduced Leakage Current in FinFETs exhibit significantly reduced subthreshold leakage compared to planar MOSFETs. This means that FinFETs experience much lower current leakage when they are in the off state, leading to improved energy efficiency and longer battery life in electronic devices. FinFETs enable high-density integration of transistors on a chip. This is particularly important for applications requiring large memory arrays and complex circuitry. FinFETs exhibit improved subthreshold slope, resulting in better performance at low power levels and more efficient operation in low-power modes. The combination of reduced leakage current, lower supply voltage, and improved gate control contributes to improved power efficiency in FinFET-based circuits. The reduced leakage current and improved performance characteristics of FinFETs can lead to enhanced reliability and longer device lifespan.

3 Design of 6T SRAM using FinFET

Because of its speed and reliability, the six transistors SRAM cell is a vital component in digital memory architecture and is frequently utilized in cache memory. It is made up of six transistors placed in a flip-flop arrangement. Six transistors are arranged into two access transistors and cross coupled inverters in the 6T SRAM cell. The data is stored in the SRAM cell using Cross-Coupled Inverters, also known as Storage Nodes. A PMOS and an NMOS transistor are linked in series to form each inverter. Gate-to-gate and drain-to-drain connections are made between these transistors. Data is read from and written to the storage nodes using the access transistors. Each storage node is coupled to one of the two access transistors. The storage nodes can read and write data thanks to these transistors. Read and write operations are performed by the 6T SRAM cell. The wordline (WL) attached to the access transistor's gate is triggered during the read operation, which reads the data that has been stored in the SRAM cell. This activates the access transistor, enabling the bitline (BL) to read data from one of

the storage nodes. The write operation involves writing data into the SRAM cell, driving the bitline (BL) to the required value, and activating the wordline (WL). Depending on the data being written, they modify the state of one of the storage nodes. The benefits are 6T SRAM cells' high operating speed allows for quick read and write access times, which makes them a good choice for cache memory. Because of the cross-coupled inverters' stability, the data contained in the 6T SRAM cells is stable and doesn't need to be refreshed on a regular basis, unlike DRAM cells.

Low Power Consumption is compared to DRAM cells, SRAM cells consume less power because they don't need refreshing. Additionally, 6T SRAM cells have lower leakage compared to some other SRAM designs. The drawbacks are Large Area with each 6T SRAM cell requires six transistors, leading to a larger area compared to some other SRAM cell designs, like 4T or 1T DRAM cells. 6T SRAM cell design is more complex due to the need for two cross-coupled inverters and two access transistors. During a read operation, the stored data can be disturbed due to the read operation itself. This can lead to potential errors if not managed properly.

A conventional 6T SRAM as shown in figure 2 cell is a fundamental memory element used in digital integrated circuits, especially in cache memory due to its stability and speed. It consists of six transistors organized in a specific configuration to store and retrieve a single bit of data. The conventional 6T SRAM cell is a crucial memory element in modern integrated circuits. Its stability, speed, and low power consumption make it suitable for applications where fast and reliable data storage is required, such as cache memory in CPUs and processors. The conventional 6T SRAM cell is a common type of memory cell used in integrated circuits, particularly in cache memories. It's called a "6T" cell because it's composed of six transistors. The 6T SRAM cell provides advantages in terms of stability and speed but comes with some drawbacks such as relatively larger area consumption per bit compared to other memory cell designs. Additionally, it requires more power during read and writes operations compared to DRAM cells.

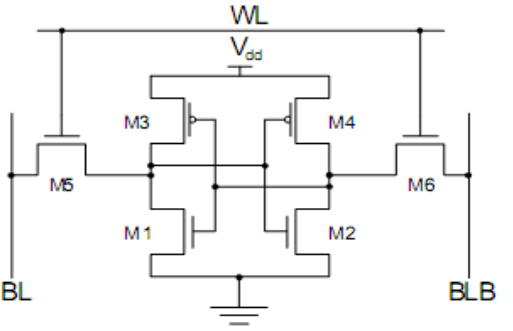

Fig. 2. Conventional SRAM 6T cell

The conventional SRAM 6T cell, while widely used and beneficial for certain applications, also comes with several drawbacks Area consumption, power consumption, complexity, read disturb, write stability, cell leakage and limited scalability. These drawbacks, chip designers often need to make trade-offs between

using SRAM for its speed and stability and using other memory types (such as DRAM) that offer higher density at the expense of some of SRAM's benefits.

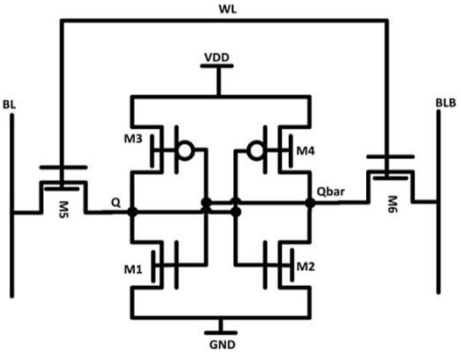

Fig. 3. Proposed FinFET based SRAM 6T Cell

Figures 3 and 4 depict the proposed FinFET based SRAM 6T cell design and its layout diagram, respectively. When designing a 6T SRAM cell, FinFET technology can have a number of benefits over conventional planar transistor technology. A kind of 3D transistor design that offers increased performance and power efficiency is called a finFET. When integrated into the 6T SRAM cell design, FinFET technology can enhance various aspects of the memory cell's operations. It's important to note that while FinFET technology offers several advantages; its adoption also comes with design challenges and increased manufacturing complexity. Engineers need to optimize the design and layout of the SRAM 6T cell to fully harness the benefits of FinFET technology while addressing potential limitations.

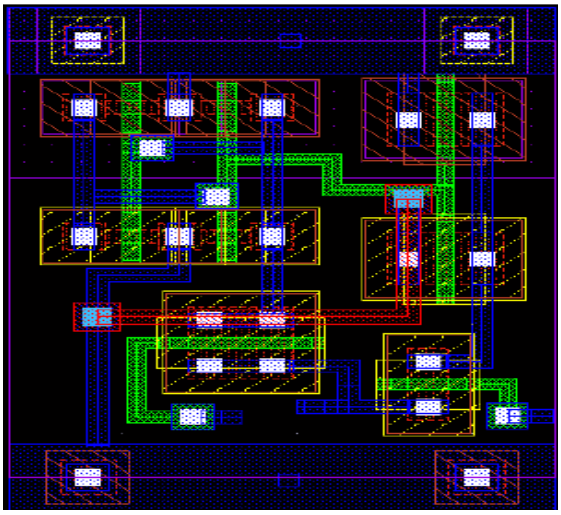

Fig. 4. Layout of 6T SRAM Cell

4 Result Analysis

When designing a 6T SRAM cell using FinFET technology instead of conventional

CMOS technology, several improvements and advantages can be achieved. Here are some of the potential results and benefits. The average power consumption during SRAM read and write operations is influenced by various factors, including the supply voltage, clock frequency (if applicable), access patterns, and the specific SRAM cell design. During read operations, the power consumption is primarily due to the internal circuitry that facilitates data retrieval. Write operations tend to consume more power because of the need to charge or discharge the cell's storage nodes, which involves changing the state of transistors. Overall, the average power consumption during SRAM read and write operations is an important consideration in modern electronics design, especially in battery-operated devices where minimizing power consumption is crucial for extending battery life. Design strategies, such as optimizing cell architectures, using low-power circuit techniques, and implementing advanced power management strategies, are employed to reduce the average power consumption of SRAM operations.

Table 1. Comparison between CMOS and FinFET

Performance parameters	CMOS	FinFET	% change in FinFET compare to CMOS
Average Power in write operation	124µW	8.76µW	92.92% reduction
Average Power in read operation	886.17nW	19.66nW	97.5% reduction

Improved Power Efficiency in FinFET technology generally offers lower leakage currents compared to CMOS technology. This leads to reduced static power consumption in the 6T SRAM cell, resulting in improved power efficiency, especially in standby modes. The improved switching speed of FinFETs can lead to faster read and write operations in the 6T SRAM cell. This translates to reduced access times, enhancing overall memory performance. FinFET technology's ability to scale down to smaller feature sizes allows for higher memory cell density on a chip. The improved control over current flow in FinFETs can lead to enhanced stability in the 6T SRAM cell. This can help mitigate issues like read disturb, write instability, and other reliability concerns. Reduced Area Consumption while FinFET technology can be slightly more complex to manufacture, its better area efficiency compared to planar CMOS can lead to smaller memory cell sizes, contributing to overall chip area reduction. Higher Performance-Per-Watt with the combination of improved power efficiency and faster switching speed results in higher performance-per-watt metrics. This means that the FinFET based SRAM 6T cell can deliver better performance levels while consuming less power compared to a CMOS-based cell.

5 Conclusions and Future Scope

In conclusion, while the advantages of using FinFET technology for designing a 6T SRAM cell in an 18nm process node are compelling, it's important to conduct a thorough analysis considering all factors. Depending on the application's priorities, power efficiency, performance, density, and long-term scalability may be decisive factors favoring the use of FinFETs. However, the potential increase in manufacturing

complexity and cost, as well as the need for careful design and testing, should also be taken into account. Ultimately, the decision should be based on a comprehensive evaluation of the specific project's requirements and constraints. FinFET technology has shown significant promise in improving the performance, power efficiency, and scalability of integrated circuits. As we look to the future, several areas hold substantial potential for the continued development and application of FinFET technology. However, as with any technological development, challenges will need to be addressed, including manufacturing complexity, process variability, and design considerations. Nonetheless, the prospects for FinFET technology remain promising as it continues to evolve and shape the landscape of semiconductor design and innovation. To conclude that 6T SRAM designed with FinFET technology is better than a CMOS design in an 18nm process node depends on a variety of factors, it's important to consider In future, the proposed design can be used in low power and high speed embedded memory applications.

6 References

1. Suman, J.V., Cheepurupalli, K.K., Allasi, H.L., 2022. Design of Polymer-Based Trigate Nanoscale FinFET for the Implementation of Two-Stage Operational Amplifier. International Journal of Polymer Science, 2022, pp. 1-12.
2. Gul, W., Shams, M., Al-Khalili, D., 2023. FinFET 6T-SRAM Compute-in-Memory Targeting Low Power Neural Networks Operations. In: IEEE International Symposium on Circuits and Systems, Proceedings (pp. 1-4), IEEE Press USA.
3. Nemati, S.H.H., Eslami, N., Moaiyeri, M.H., 2023. A Hybrid SRAM/RRAM In-Memory Computing Architecture Based on A Reconfigurable SRAM Sense Amplifier, IEEE Access, 11, pp. 72159-72171.
4. Parihar, S.S., Thomann, S., Pahwa, G., Chauhan, Y.S., Amrouch, H., 2023. 5nm FinFET Cryogenic SRAM Evaluation for Quantum Computing. In: Device Research Conference, Proceedings (pp. 1-2), IEEE Press USA.
5. Gupta, A., Chauhan, N., Prakash, O., Amrouch, H., 2021. Variability Effects in FinFET Transistors and Emerging NC-FinFET. İn: IEEE International Conference on IC Design and Technology, Proceedings (pp. 1-4), IEEE Press Germany.
6. Parihar, S.S., Van Santen, V.M., Thomann, S., Pahwa, G., Chauhan, Y.S., Amrouch, H., 2023. Cryogenic CMOS for quantum processing: 5-Nm FinFET-Based SRAM arrays at 10 K. IEEE Transactions on Circuits and Systems I: Regular Papers, 70, pp. 1–14.
7. Sharma, N., 2016. Ultra Low power dissipation in 9T SRAM design by using FinFET Technology. In: IEEE International Conference on ICT in Business Industry & Government, Proceedings (pp. 1-5), IEEE Press Indore.
8. Srinivasa Rao, P.K., Suman, J.V., 2013. Low Power Design of A SRAM Cell for Embedded Memory. International Journal of Research in Computer and Communication Technology, 2, pp. 1222-1228.
9. Verma, S., Tripathi, S.L., Bassi, M., 2019. Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications. İn: Devices for Integrated Circuit, Proceedings (pp. 84-88), IEEE Press India.
10. Kim, S.H., Fossum, J.G., 2007. Design Optimization and Performance Projection of Double-Gate FinFETs with Gate-Source/Drain Underlap for SRAM Application. IEEE Transcation on Electron Devices, 54, pp. 1934-1942.
11. Avanija, J., K. E. Kumar, Ch Usha Kumari, G. Naga Jyothi, K. Srujan Raju, and K. Reddy Madhavi. "Enhancing Network Forensic and Deep Learning Mechanism for

Internet of Things Networks." (2023).
12. Suman, J.V., Sukanya, D., Kavya, P., 2023. Simplified Bilayer TFETS with Oxide and Group-IV Semiconductor for P-Channel Operation. International Journal of Scientific Research in Engineering and Management (IJSREM), 7, pp. 1-9.
13. Suman, J.V., Siri Chandana, N., 2023. A Review of Machine Learning-Based Device Modeling and Performance Optimization for FinFETs. International Journal of Scientific Research in Engineering and Management (IJSREM), 7, pp. 1-10.