FinFET based Design and Performance Evolution of Multiplexers

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Abstract. A multiplexer is a combinational logic designed to switch one of multiple input lines to a single common output line. Multiplexer is used in various designs in Very Large Scale Integration and Digital Signal Processing applications. FinFETs are emerging transistors that can work in the nanometre range to overcome these short-channel effects. In this paper, a FinFET technology-based multiplexer is proposed and designed using the Cadence Virtuoso Tool. Furthermore, the proposed design is compared with conventional CMOS and existing FinFET designs. From the results table, the proposed design gives low power dissipation, reduced time and Power Delay Product (PDP) compared to the existing designs. This design also reduces the area utilized for low-power applications by reducing the number of transistors.

Keywords: Cadence Virtuoso, FinFET, Multiplexer, Short Channel Effect, Spectra Simulator

1 Introduction

The increase in the requirements of complex operations on a single chip has led the semiconductor circuit designing process to various difficulties and challenges [1]. Over the last few decades, to overcome these difficulties, the physical length of planar MOSFET is shortened to improve their efficiency of power consumption and speed. The decrease in the physical length of planar silicon MOSFET resulted in the

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increase of leakage current and the dissipation of leakage power due to effects of short channel [2]. The further scaling in bulk MOSFET will lead to more unwanted power dissipation. To overcome this second-order effect FinFET technology is introduced. The abbreviation of FinFET is Fin Field Effect Transistor. The other name for FinFET is multi-gate MOS transistors. In FinFET, the transistor substrate can be formed by wrapping the conducting channel by a silicon wafer. FinFET is a Nonplanar Dual Gate Transistor used in Silicon Architecture which consists of very large computational density. The problems faced by the MOSFET are overcome by FINFETs. FINFET it a multi gate field affect transistor which is further scaled down than the MOSFET. FINFET has similar properties to that of a conventional transistor but has some advantages on CMOS.

FINFETs consume less area than the MOSFETs. Since the gate wrapped around the channel, the gate has more control over the drain resulting in fast operation and less power dissipation. FINFET also requires less supply voltage to operate. The bulk CMOS designs have the drawbacks like high leakage current, less channel controllability and manufacturing with low package density. These drawbacks of bulk MOSFETs are overcome by Double-gate FINFETs [3].

1.1 Multiplexer

The multiplexer, sometimes also referred as a data selector is the combinational circuit. A 2^n:1 multiplexer has 2^n input lines and a single output line with n selecting lines. The multiplexer output is decided by the selecting lines. Multiplexers can also be used to implement Boolean functions of multiple variables and are used extensively in many VLSI applications, communication, image processing, video editing, and circuit design [4]. The main consideration of FinFET technology is to maintain less power consumption. FinFET technology can be used to minimize the power consumption in a multiplexer [5].

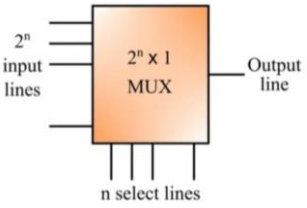

Fig. 1. N to1 multiplexer

2 Literature Survey

2.1 Multiplexer using CMOS Technology

M. Suresh et.al well discussed conventional CMOS logic based implementation of 4:1 MUX. It is observed that the transistors count is more in CMOS logic. In this paper, it is discussed that conventional logic will dissipate more in accordance with the power consumed. Using Tanner T-spice tool simulation results of multiplexer using CMOS logic are compared with other low power techniques and found that the power dissipation is higher in CMOS logic. The delay between the input and output is also more [6]. The conventional CMOS based 4:1 multiplexer is shown in figure 2.

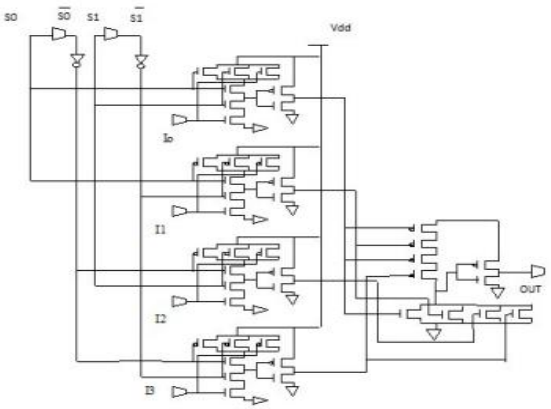

Fig. 2. Conventional CMOS based 4:1 Multiplexer

2.2 Multiplexer using GDI Technology

In this it is also discussed that GDI technique can be used to lower the power dissipation and can obtain better results in time delay. 6 transistors are used in this design of GDI based 4:1 multiplexer which in turn reduced the area up to great extent. The major difference in GDI when compared to CMOS is that it consists of 3 inputs. The GDI is efficient in power delay and low power. But the main drawback is it requires twin well CMOS process to implement the GDI cell.

2.3 Multiplexer using DPTL

Yalla Hareesh et.al proposed Dual Pass Transistor Logic (DPTL) based 4:1 MUX design. In this paper, 4:1 MUX design using the DPTL technique is compared with other techniques like CMOS and Transmission Gate (TG). The basic structure of DPTL consists of pMOS and nMOS transistors connected in parallel. The logic function in DPTL is generated by switching NMOS and PMOS, VDD, and GND. It is observed that the transistors count in DPTL is reduced approximately 4 times that of CMOS logic. Six transistors are used in the design making of MUX using DPTL. It is observed that the delay is reduced but the power dissipation is high in DPTL. In this paper, the simulations are done using Tanner EDA and the simulation results are compared with other techniques [7]. FinFET-based DPTL design is proposed which also has high power dissipation but the delay is reduced comparatively to the conventional DPTL logic.

2.4 Multiplexer using FinFET

S.Sujata et.al proposed a 4:1 multiplexer using 32nm FinFET technology with 20 transistors [8-11]. Using the Cadence tool, the simulations are done and the power and delay parameters are calculated and compared with the design which is not based on FinFET. It also has the highest performance in terms of speed; the area is used efficiently and also reduces the short channel effects. It is observed that the provided design has reduced power dissipation and delay which is based on FinFET technology [12-15].

3 Proposed Methodology

3.1 FinFET based 4:1 multiplexer using 6 transistors

On reviewing the existing technologies that can implement the required 4:1 multiplexer with well reduced power dissipation and less time delay, a design is proposed using 18nm technology with 6 transistors and it is observed that it has less power dissipation and also consumes very less area which is more advantageous in the aspect of its physical implementation. Proposed FinFET based 4:1 multiplexer using 6 transistors is shown in figure 3.

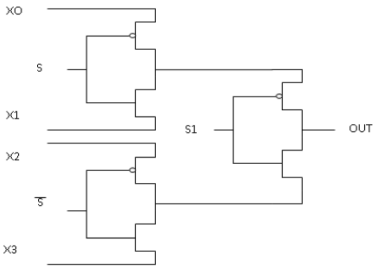

Fig. 3. Proposed FinFET based 4 to 1 multiplexer

Simulation results of proposed FinFET based 4:1 multiplexer is shown in figure 4.

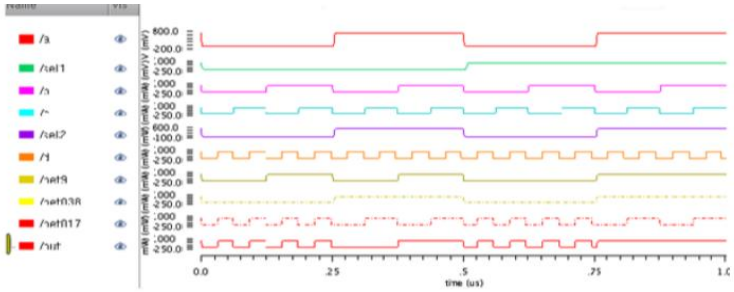

Fig. 4. Simulation results of proposed FinFET based 4 to 1 multiplexer

4 Results

The performance comparison of various multiplexers is shown in table I. In this performance comparison considered number of transistors count, power, delay and PDP parameters. From the results comparison table I, it is clearly observed that the proposed FinFET based 4:1 multiplexer shows better performance as compared with conventional CMOS, GDI and other existing FinFET designs.

Table 1. Performance comparison of various 4:1 Multiplexers

Multiplexer	Number of Transistors	Power (μw)	Delay (Psec)	Power & Delay Product (PDP)
CMOS 29T Multiplexer [6]	29	26.31	1.124	29.56
Mux using GDI [6]	6	3.596	0.206	0.74
Mux using DPTL [7]	6	14.24	-	-
FinFET (DPTL)	6	7.054	0.197	1.38
FinFET (32nm) [8]	20	8.557	0.908	7.76
FinFET (18nm)	20	5.467	0.766	4.18
FinFET (Proposed)	6	1.260	0.166	0.209

5 Conclusıons and Future Scope

The proposed FinFET based 4:1 MUX using 6 transistors was designed and simulated using Cadence Virtuoso tool. The simulation results were compared with existing technologies like conventional CMOS logic, GDI logic and existing FinFET based designs. It is observed that the power dissipation is reduced by 85 percentages and the delay is reduced by 81 percentages in the proposed FinFET based 4:1 MUX when compared to existing FinFET based designs. Finally, we concluded that the proposed FinFET based multiplexer has better PDP than other existing technologies. In future, this proposed FinFET based multiplexer can be used in various low power applications like communication with reduced power dissipation and delay.

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