Design of 7-bit 16-MSample/s Low Supply Low Power Digital-to-Analog Converter*

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Abstract. In this paper, a 7-bit 16-MSample/s current-steering CMOS digital-to-analog (D/A) converter is presented. Current steering architecture consists of binary-weighted cells, the post-layout simulation results show that the SFDR and ENOB are more than 52.50 dB and 6.97 bit with a 1.984MHz input. The integral nonlinearity (INL) and differential nonlinearity (DNL) are both better than 0.16 LSB. The total power consumption is 93 μW.

Keywords: 7-bit DAC; low supply; low power; current-steering.

1 Introduction

The evolution in the field of wireless communications and the mixed-signal area, especially in wireless local area network (WLAN) and mobile communication, pushes the designer to put an increasing amount of efforts in the integration of digital and analog system on one chip, consequently, the data converter between these two systems become one of the most challenging blocks to design. High performance digital-to-analog (D/A) converter usually found applications in the area of, e.g., HDTV, GSM and CDMA. Although these areas require different performance of D/A converter, the low supply, low power is still the trend of the COMS D/A converter design, because the modern communication system cares more about the power consumption.

In the next section, the D/A converter's basic operation principles will be discussed. In section 3, the different building blocks of the current-steering D/A converter are covered in detail, including the benefit and the drawback of different topology, and the topology selection. The simulation results will be given at last.

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2 DAC Architecture

Today's designer usually focuses on two directions, one is high-speed and high-accuracy, the other is low power consumption and low-cost [1] [2]. Compared with other structures, current-steering structure is frequently adopted due to its inherent high-performance [3]. This paper also uses current-steering structure. Base on sample frequency and the area of layout, we choose the binary-weighted structure.

Fig.1 shows the architecture of the 7-bit current-steering D/A converter, which consist of input driver, synchronous latch, current cells, and a bias circuit. The input driver is segmented into 8 parts, which correspond, respectively, to 7 digital inputs and clock, and it can also generate complementary signals. The synchronous latch retimes the control signals from the input driver to minimize the timing error, and the timing synchronizations in this circuit are controlled by the clock.

Finally, the bias circuit generates bias voltage for 127 current source arrays to generate currents by a current reference. All currents, at last, flow into two resistors to form a fully differential signal through the current switching array controlled by the control signals.

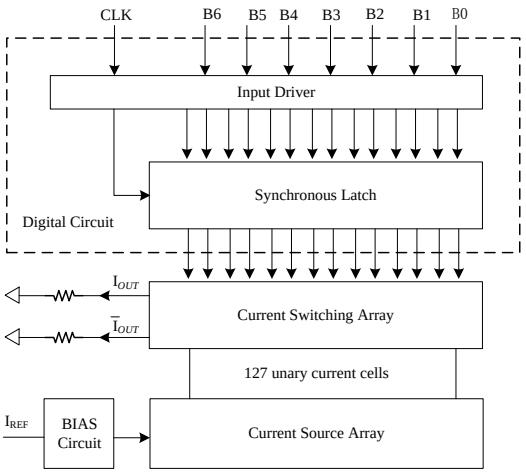

Fig.1 7-bit current-steering DAC architecture

2.1 Bias circuit

In lots of 0.18μm CMOS D/A converter designs, The supply is often set to 1.8V, but in order to reducing power consumption, in this paper, the supply is limited to

1V, consequently, many high performance structures can't be used because of the low supply. This situation certainly makes the design full of challenge.

Bias circuit provides the bias voltage for current source arrays, and it is the key module that decides the precision and stability of the current source arrays, its performance can also influence the performance of the D/A converter.

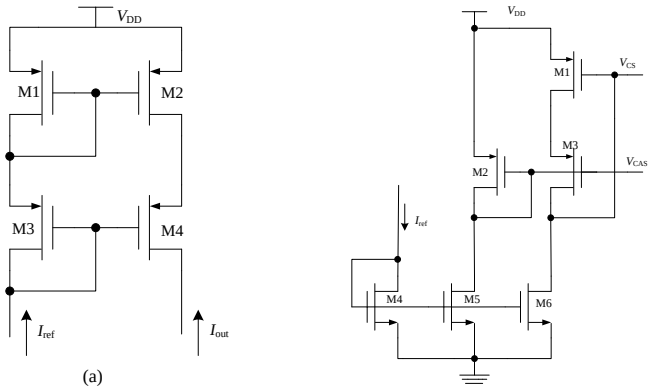

Fig.2 Two kinds of cascode current mirror (a) The traditional cascode current mirror (b) The improved cascode current mirror

In order to ensure the performance of the current source, high output impedance is needed, which can improve the performance of the D/A converter. Finite output impedance will not only limit the improvement of integral nonlinearity (INL), but limit the improvement of SFDR [4]. The traditional cascade current mirror is shown in Fig. 2(a), it provides high output impedance and constant current, which not only eliminates the channel length modulation effect, but also shields influences of output voltage variation. The defect of this architecture is that it is not suitable for the low supply design owe to its cascaded structure. The improved one, shown in Fig. 2(b), can solve the problem by adding M2 and M5.

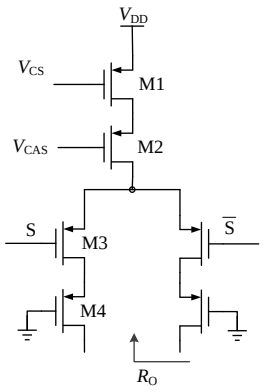

Fig.3 Current cell

2.2 Current cell

The current cell is an important component for frequency-domain performances in the low supply D/A converter design. Primary design issues are usually focused on mismatches and finite output impedance. The schematic of a current cell is shown in Fig. 3. A cascode current source is chosen for its inherent high output impedance, and it can lower the glitch energy error caused by the drain voltage variation of the current source.

The output impedance of current cell can be expressed as R_O, shown in equation (1)

$$R_O = g_{m4} g_{m3} g_{m2} r_{o4} r_{o3} r_{o2} r_{o1} \tag{1}$$

Therefor we can solve the design issues mentioned above by setting the parameter reasonably. In consideration of the noise jamming, P-type MOSFETs are chosen for its lower noise jamming.

Consider the small-signal equivalent circuit shown in Fig. 4, where r_O represents the output impedance of each current source. The equivalent output impedance can be given by

$$R_{OUT} = R_L \parallel \frac{r_O}{n} \tag{2}$$

Where n is the number of current sources that are switched on, R_L is the load resistor, and the output voltage is

$$V_{\mathrm{OUT}} = nI(R_{\mathrm{L}} \parallel \frac{r_{\mathrm{O}}}{n}) \tag{3}$$

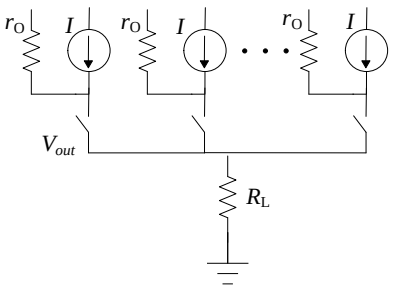

Fig.4 Current-steering array including output impedance of each current source

To obtain the INL profile, we draw a straight line through the end point of equation (3) (given by n=0 and n=N) and find the difference between equation (3) and the straight line, then the INL approximated as

$$\mathrm{INL}_n = \frac{IR_{\mathrm{L}}^2}{r_{\mathrm{O}}} n(N-n) \tag{4}$$

From equation (4) we can get the conclusion that the higher the equivalent output impedance of current source is, the smaller the INL is.

Current value setting is needed after the selection of architecture. To Reducing power consumption, we need to reduce the value of unary current, but it will also arise question that the interference from other factors e.g., supply, clock and temperature, will come to the front, as a result, the INL and SNR will seriously deteriorate. After repeated weigh, the value of unary current is set to 500nA.

2.3 Synchronous latch

The dynamic performance degradation of a current- steering D/A converter can be caused by the imperfect synchronization of the control signal at the switches and the drain-voltage variation of the current-source transistors.

To minimize these two effects, a well-designed and carefully laid out synchronized latch is needed. By placing it in front of the switches and by paying much attention to symmetrical interconnections in the layout, the difference in delay between the different paths is minimized [5]. The circuit schematic of the latch circuit is shown in Fig. 5. To avoid the both switching transistors at off state, we should shift the crossing point of switch transistor's differential control signals. The driver also performs the final synchronization. It provides two complementary signals needed at the input of the stitch transistors in the current source.

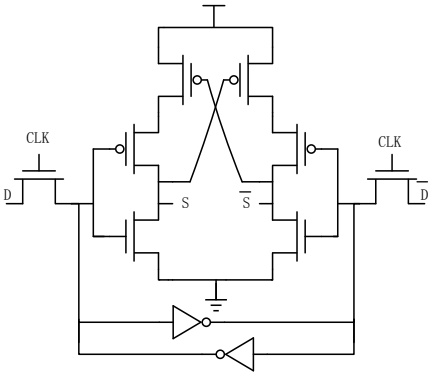

Fig.5 Synchronous latch

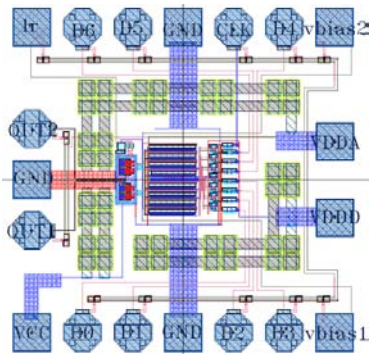

Fig.6 Layout of current-steering DAC

3 Simulation Results

The converter was fabricated in a 0.18μm CMOS technology with a 1V supply voltage and the output load resistor is 1 kilohm doubly terminated. The full-scale output voltage is 75.8 mV. Fig. 6 shows the layout of the 7-bit current-steering DAC. The active area is 0.675 x 0.675 mm^2.

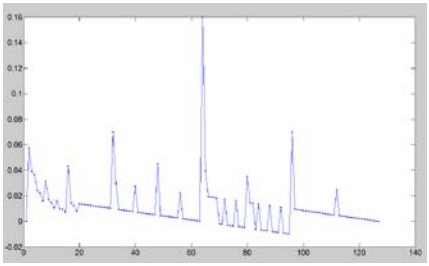

Fig.7 The INL performance

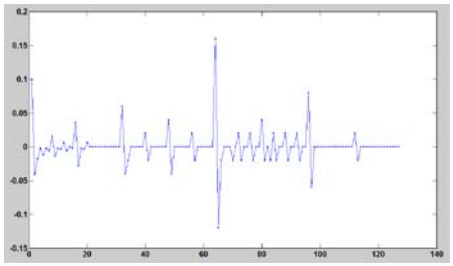

Fig.8 The DNL performance

Fig. 7 shows the INL performance of the D/A converter, and Fig. 8 shows the DNL performance of the D/A converter. The simulation results show that INL and DNL are both better than 0.16 LSB. Fig. 9 shows the output spectrum for a 1.98 MHz signal at a 16 MHz sampling rate. The SFDR is 52.5 dB and the SNR is 42.96dB.

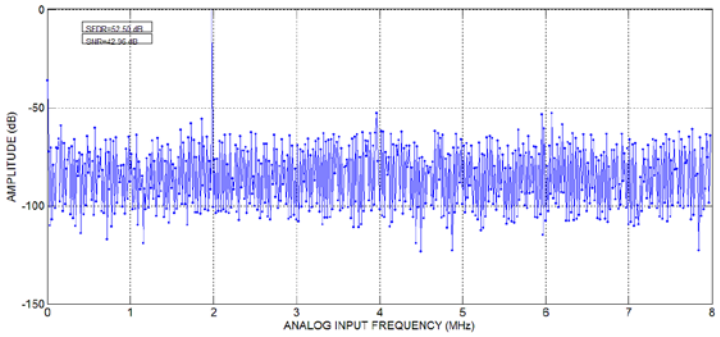

Fig.9 The output spectrum for a 1.998MHz at a 16MHZ update rate

Table 1 Summary of the DAC specifications

Parameters	Value
Process	0.18μm CMOS
Resolution	7-bit
Update rate	16 MHz
INL	<0.16 LSB
DNL	<0.16 LSB
SFDR(1.98MHz@16MHz)	52.50 dB
SNR(1.98MHz@16MHz)	42.96 dB
ENOB(1.98MHz@16MHz)	6.98 bits
Power consumption(1.98MHz@16MHz)	93 μW
Supply	1 V
Full-scale output voltage (1.98MHz@16MHz)	75.8 mV

4 Conclusion

In this paper, a 0.18μm CMOS 7-bit, 16MS/s D/A converter capable of operating at a low supply voltage of 1V is presented for wireless communications. According to the results of post-layout simulations, a SFDR of 52.5 dB and ENOB of 9.98 bits can be achieved from a full-scale output voltage of 75.8 mV. The active area is 0.675 x 0.675 mm^2.

5 Reference

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